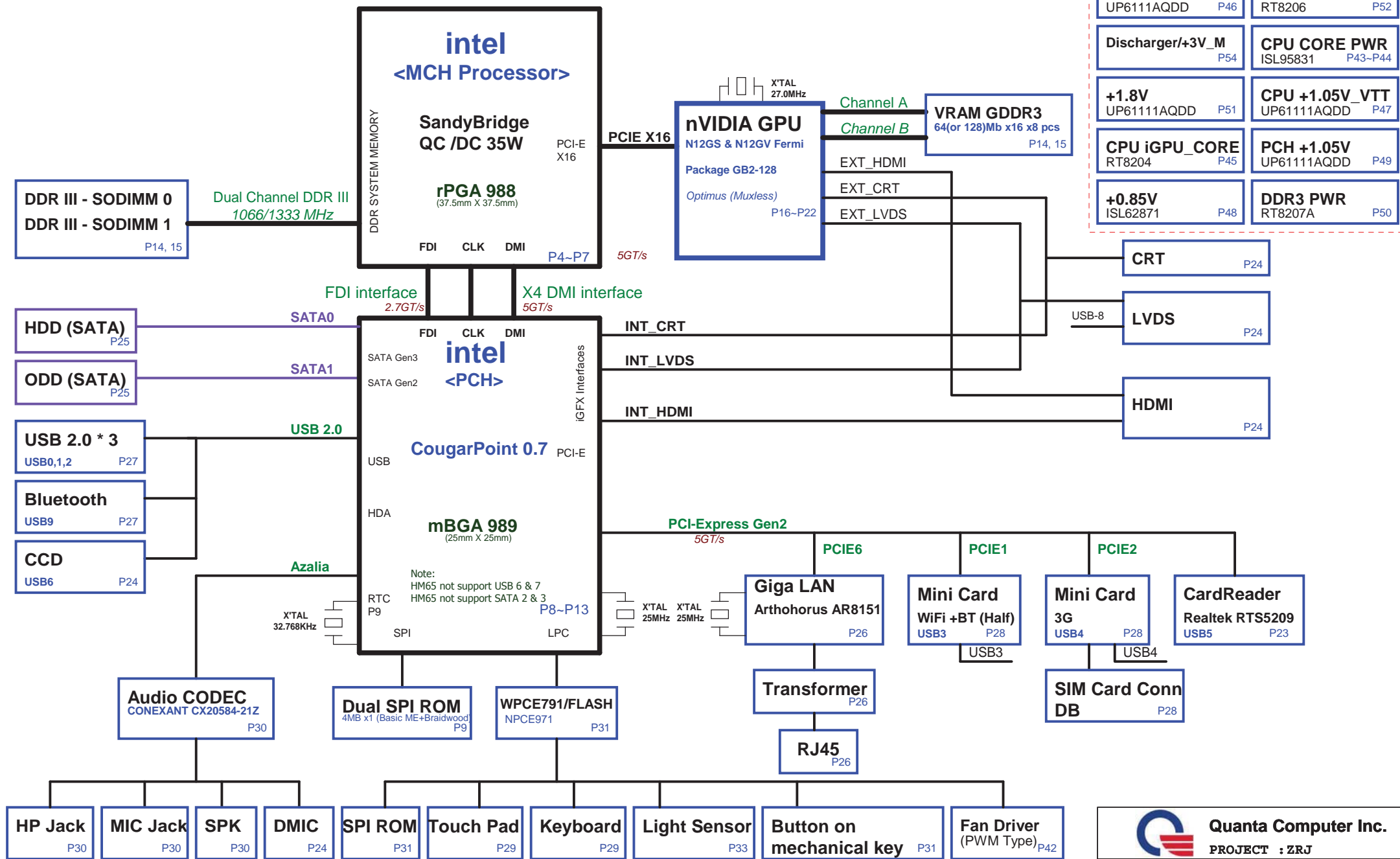
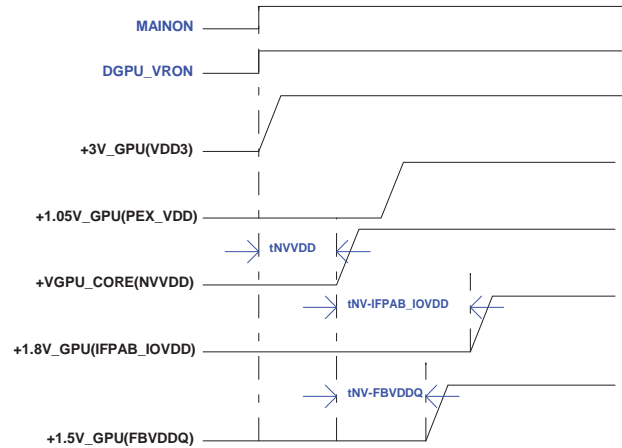


ZRJ BLOCK DIAGRAM

01



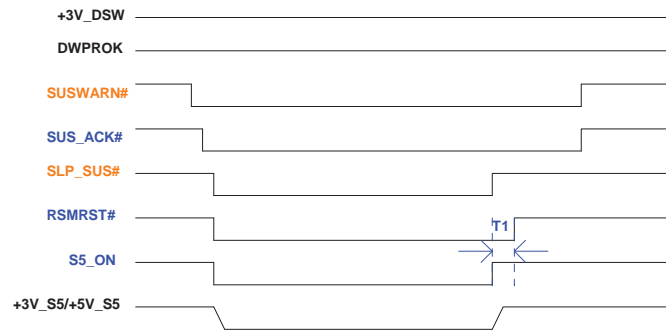
N12P-GE Power Up Sequence



N12P-GE Power up Sequence

tINVDD>0
tINV-IFPAB_IOVDD>0
tINV-FBVDDQ>0

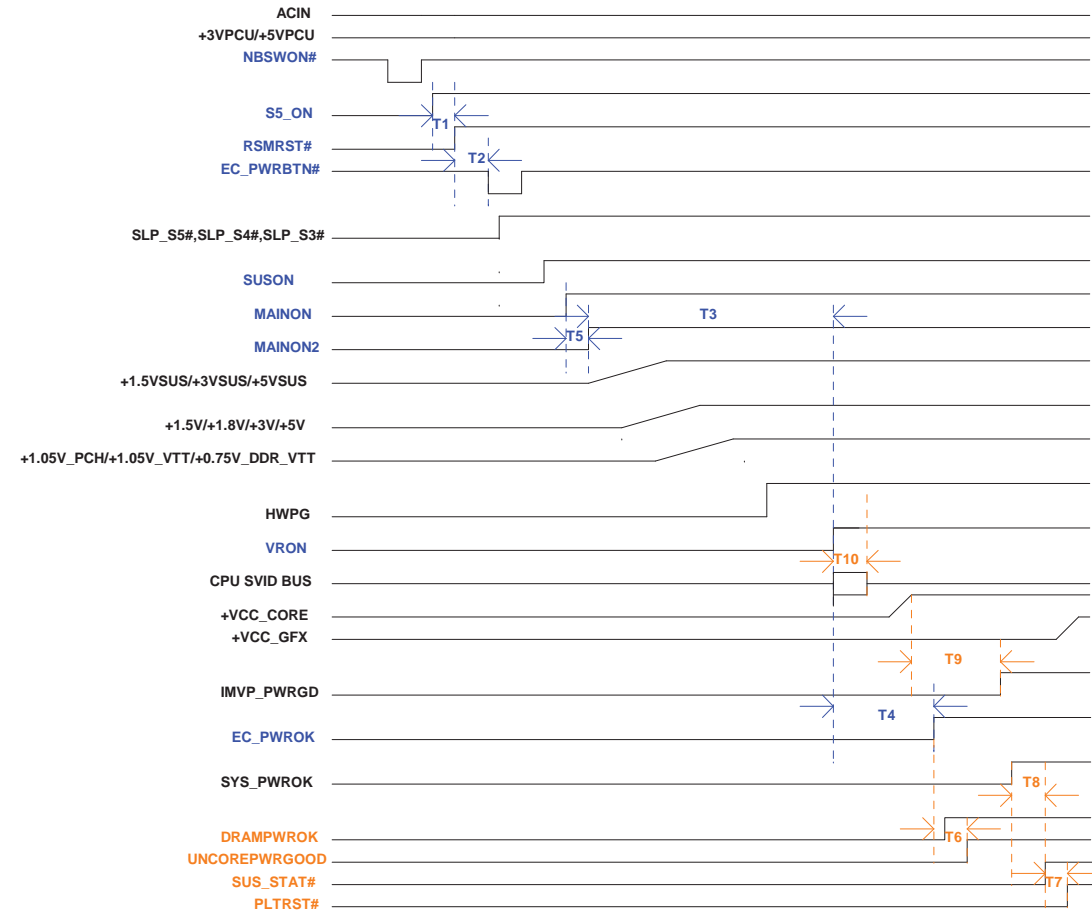
Deep S4/S5 off-on Sequence



Deep S4/S5 Sequence

T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

MS15-UMA Power-ON Sequence



System Power Sequence

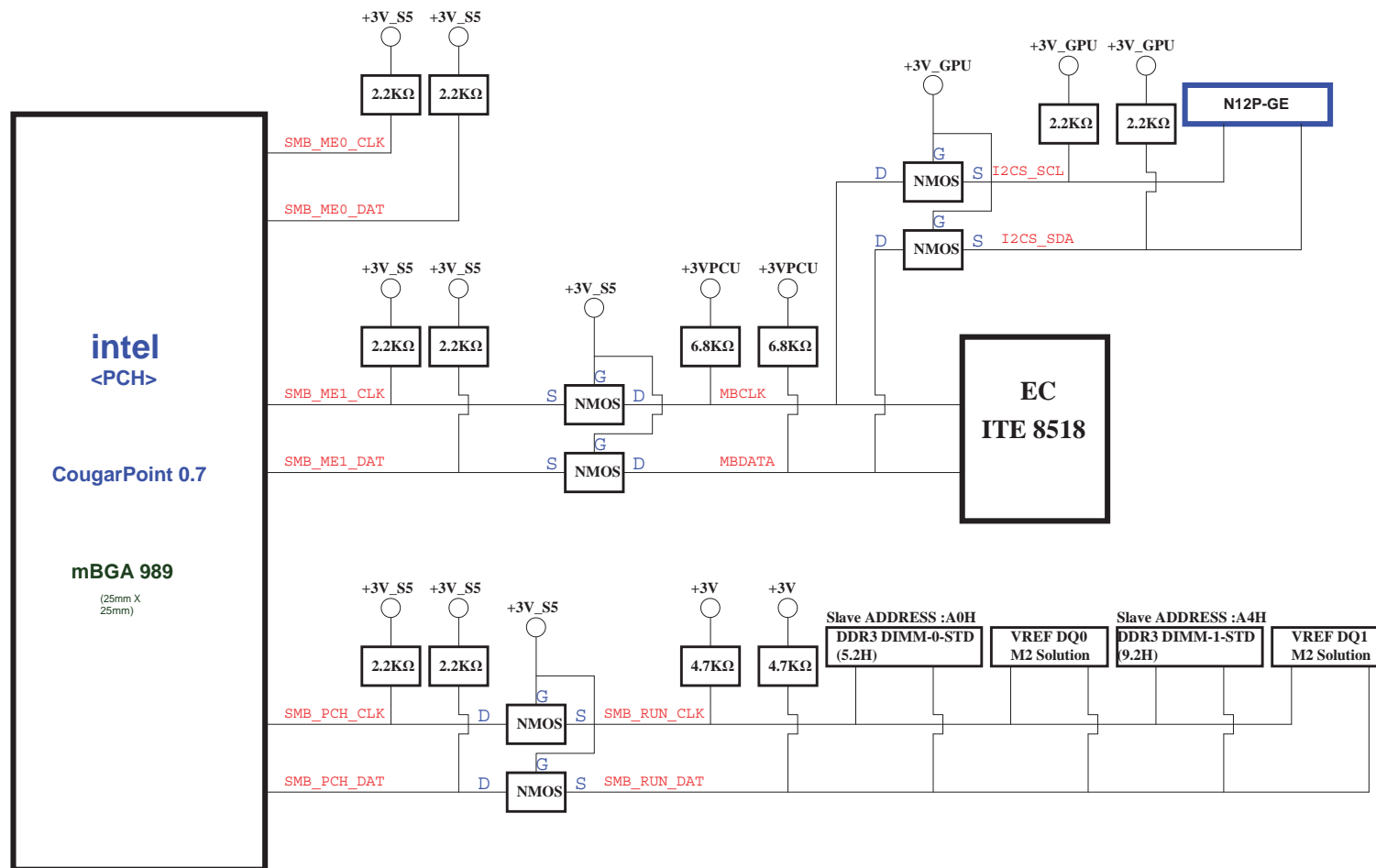
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO EC_PWRBTN# = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO EC_PWROK = 10ms (HWPG NEED TO BE HIGH at that time)
T5: MAINON TO MAINON2 = 500us
T6: EC_PWROK TO UNCOREPWROGOOD = 2ms(Min)
T7: SUS_STAT# TO PLTRST# = 60us(Min)
T8: SYS_PWROK TO SUS_STAT# = 1ms(Min)
T9: +VCC_CORE TO IMVP_PWRGD = 5ms(Max)
T10: VRON to accept SVID command. = 5ms(Max)



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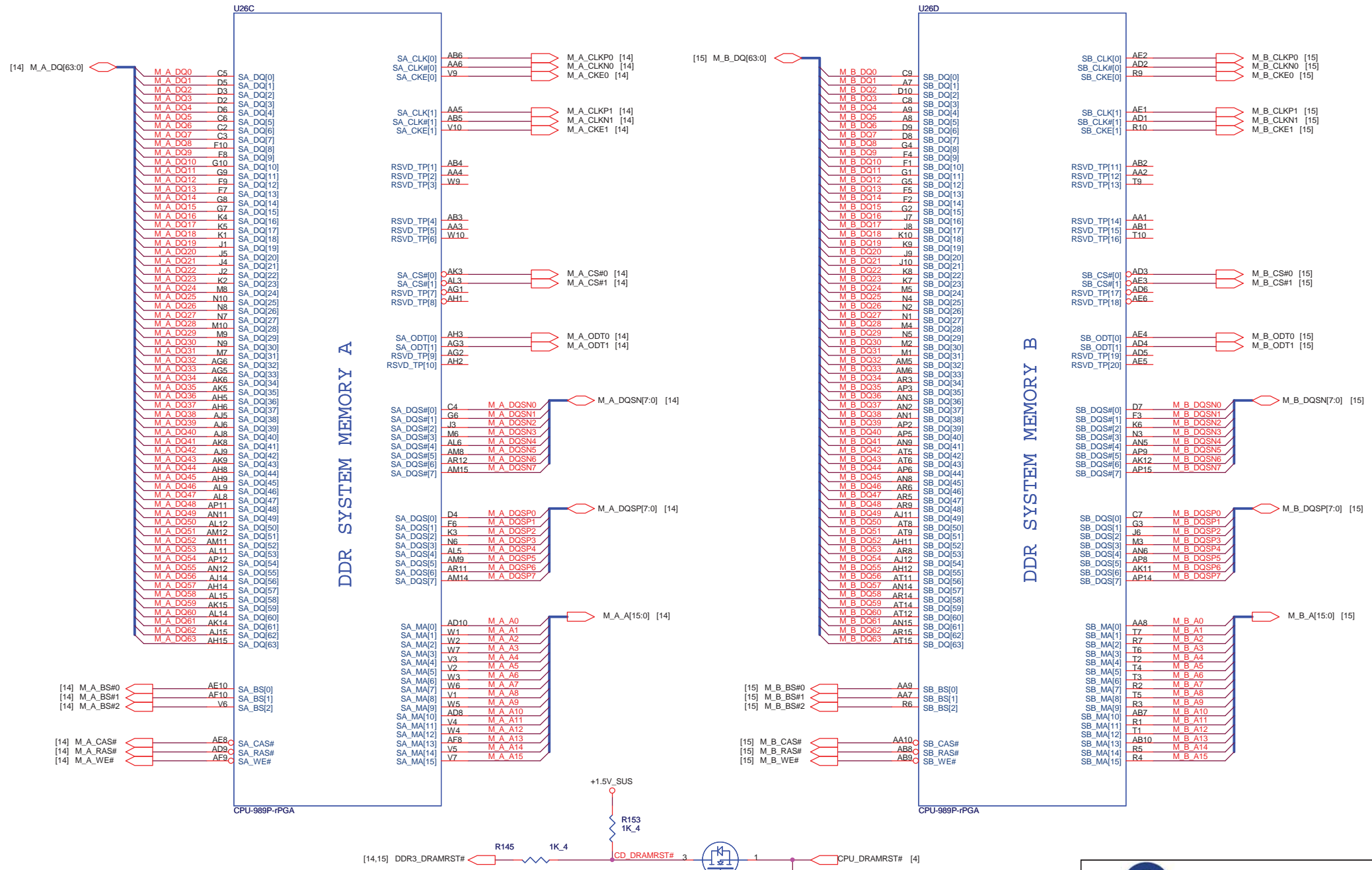
PROJECT : ZRJ

Size	Document Number	Frontpage	Rev 1A
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Sandy Bridge Processor (CLK,MISC,JTAG)

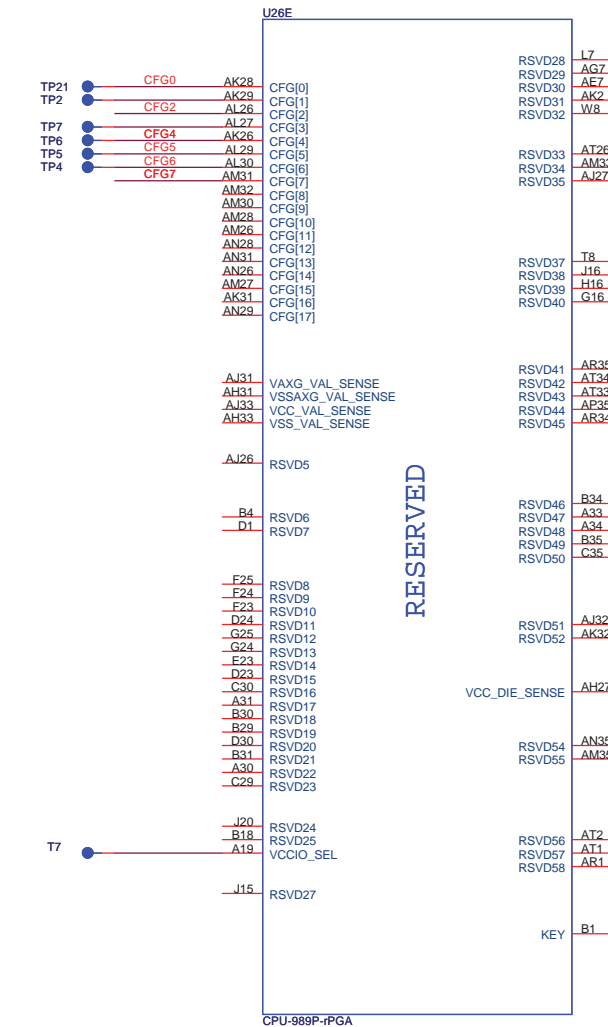
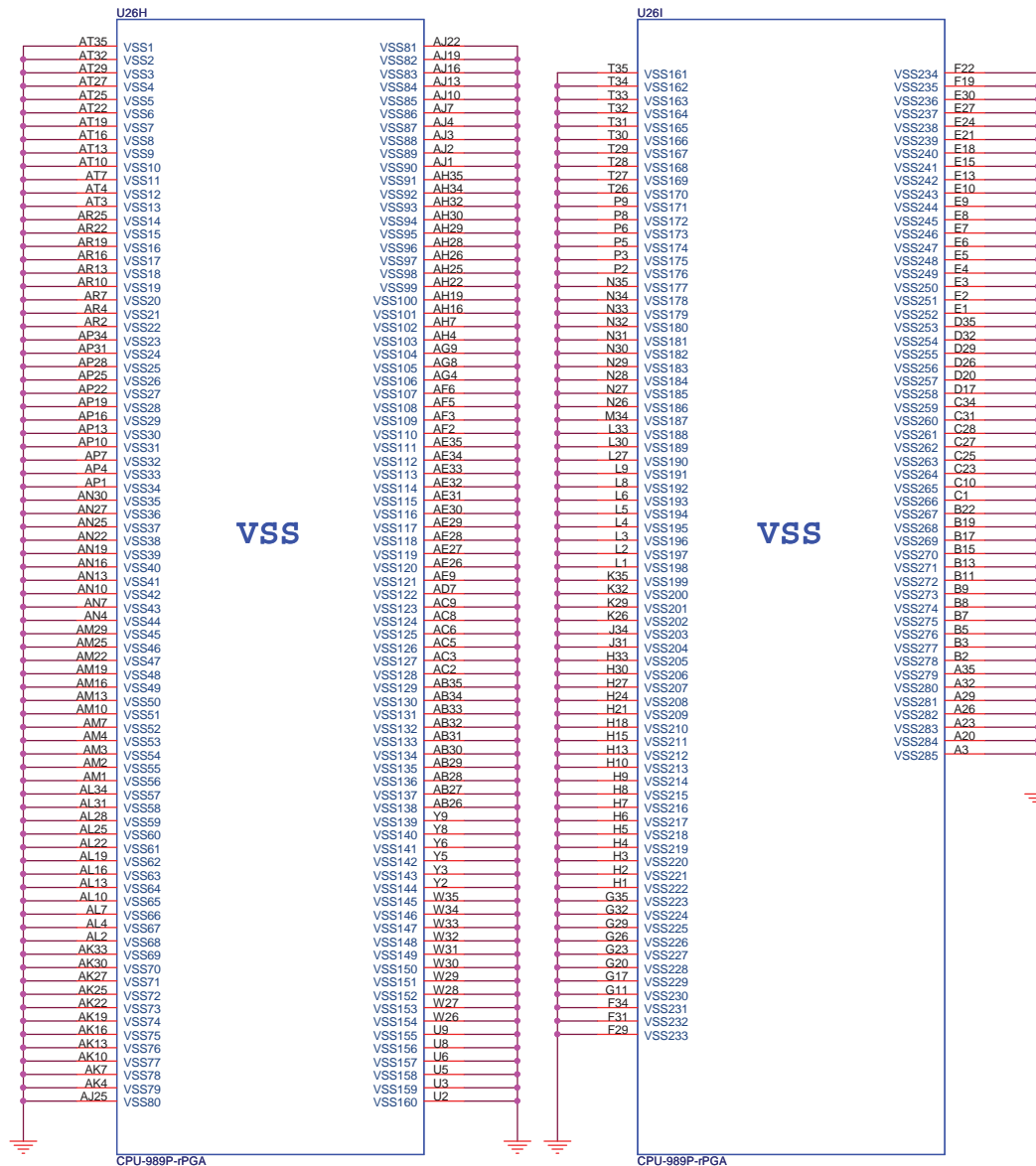
[illegible]



Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)

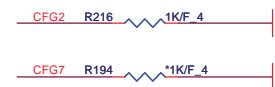
07



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)

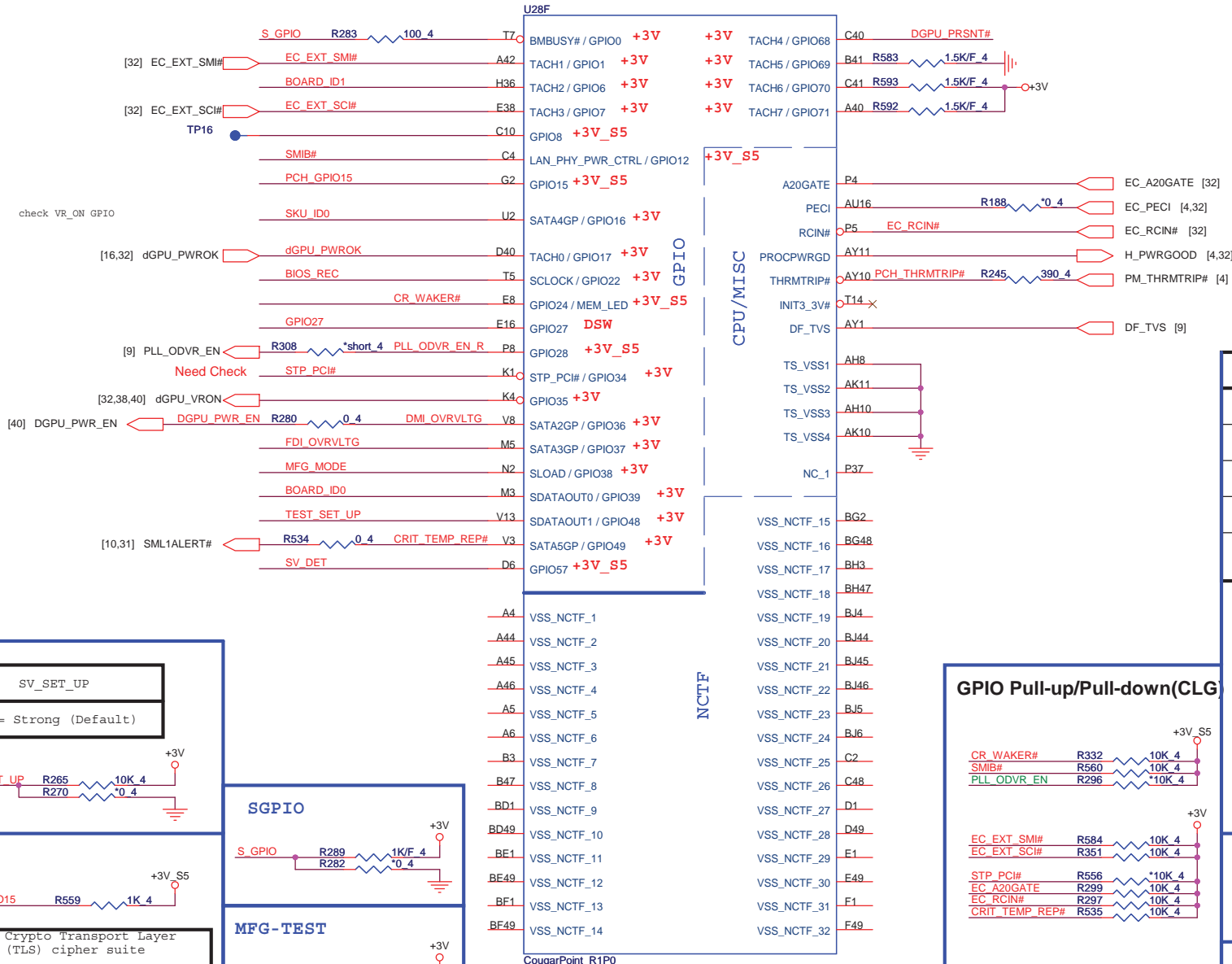
11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Size	Document Number	Rev
	Sandy Bridge 4/4	1A
Date:	Monday, December 20, 2010	Sheet 7 of 41

Cougar Point (GPIO,VSS_NCTF,RSVD)

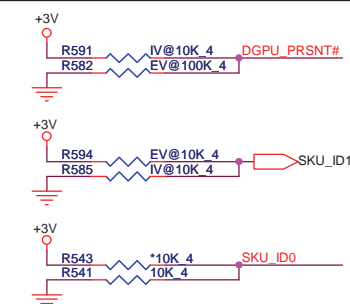
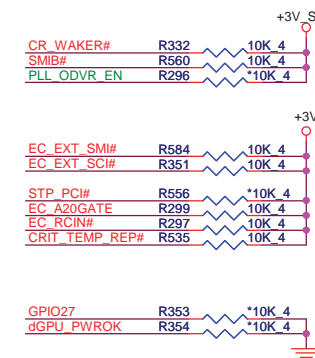
11



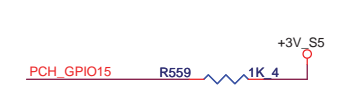
	DGPU PRSNT# (GPIO68)	SKU ID1 (GPIO64)	SKU ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	DIS/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

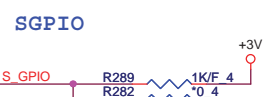
GPIO Pull-up/Pull-down(CLG)



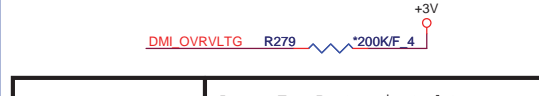
SV_SET_UP
High = Strong (Default)



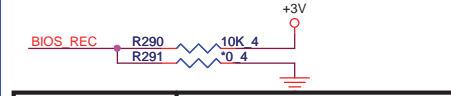
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable



FDI TERMINATION VOLTAGE OVERRIDE
Low - Tx, Rx terminated to same voltage



DMI TERMINATION VOLTAGE OVERRIDE
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

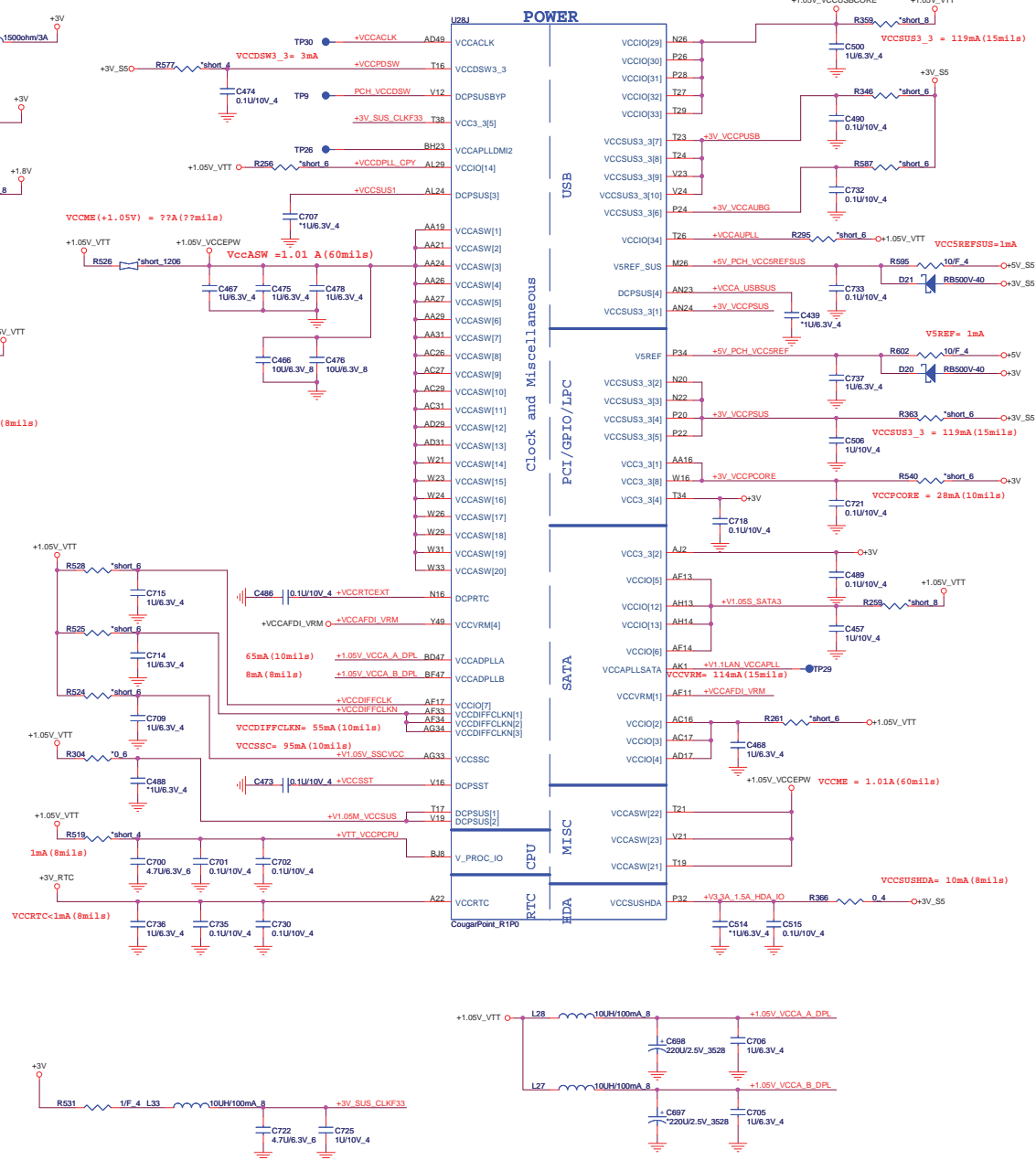


BIOS RECOVERY
High = Disable (Default)
Low = Enable

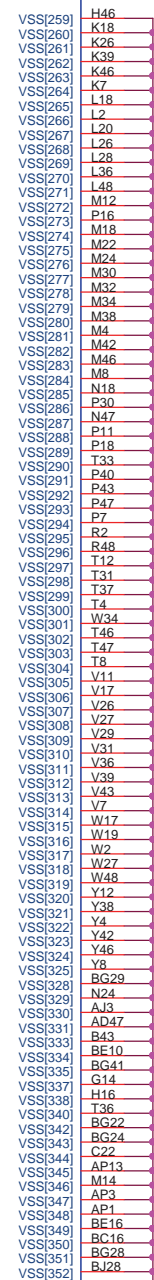
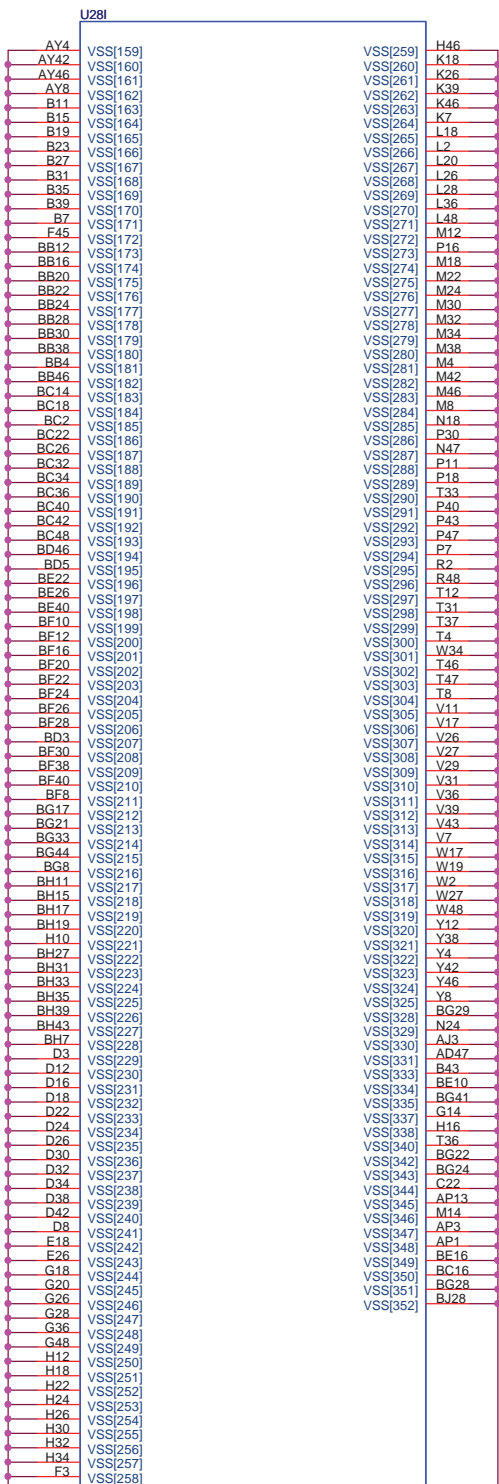
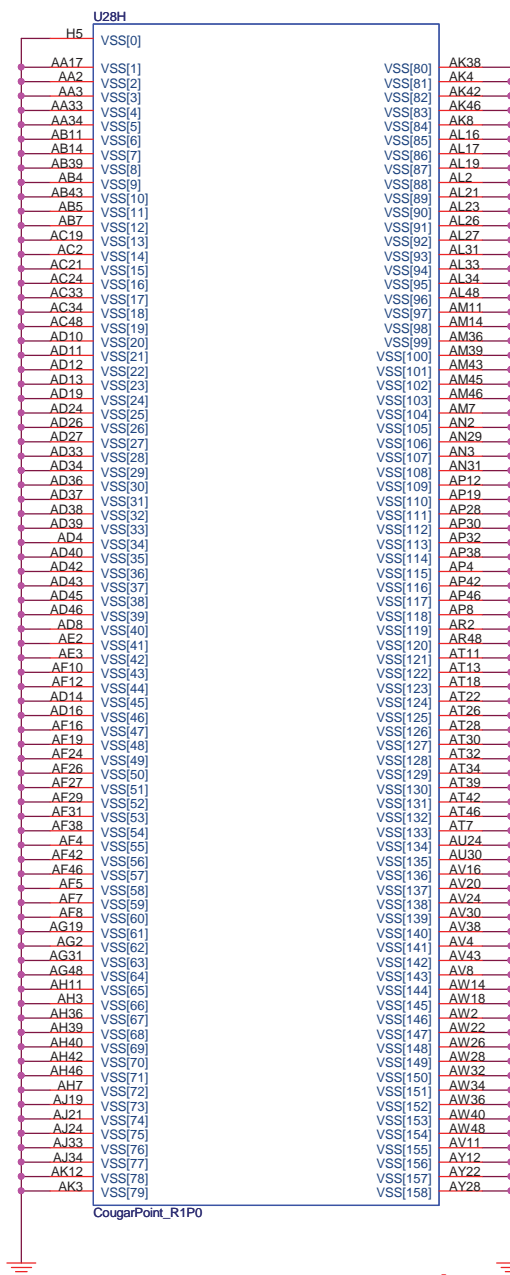
Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev 1A
Cougar Point 4/6		
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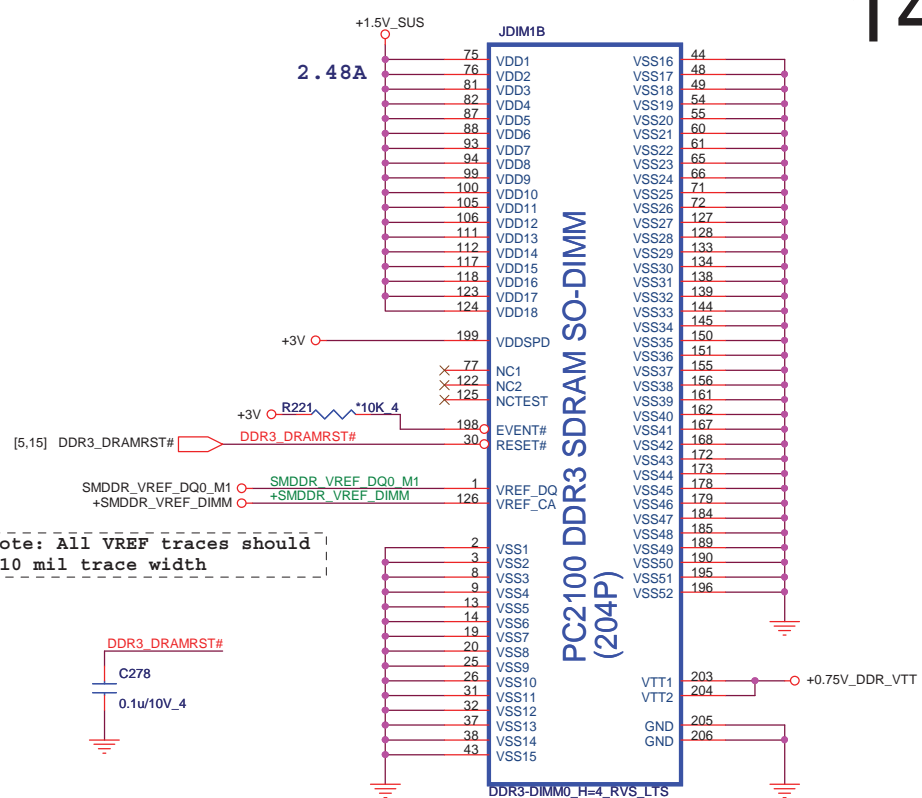
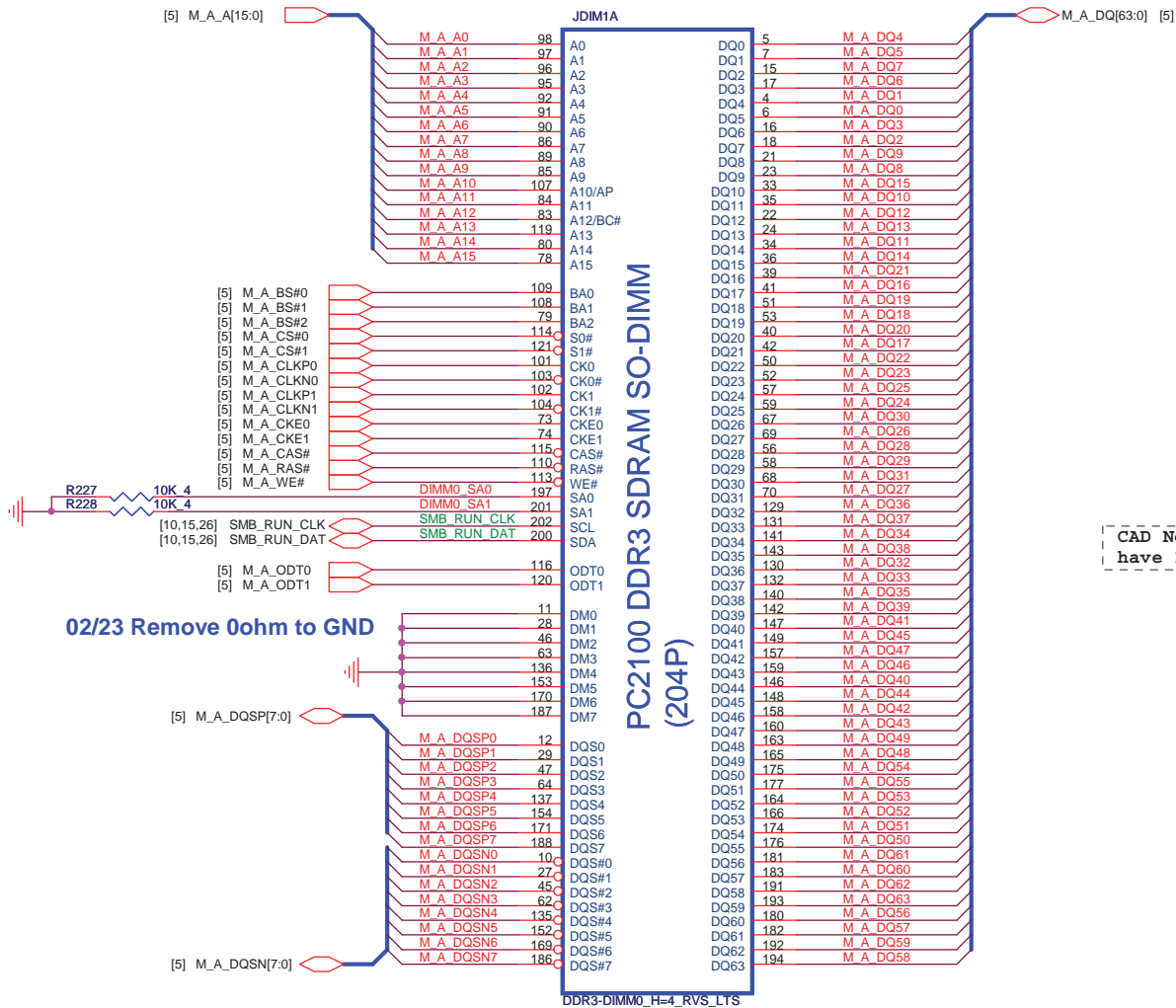
Cougar Point-M (POWER)



IBEX PEAK-M (GND)



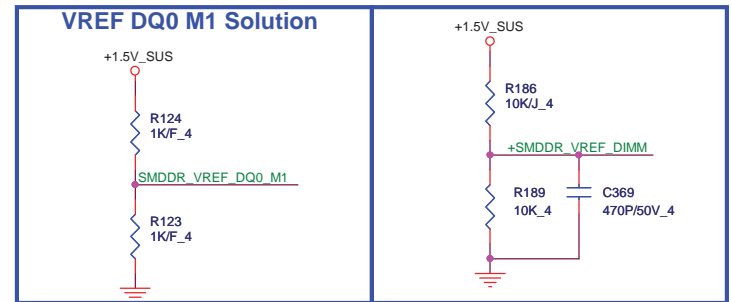
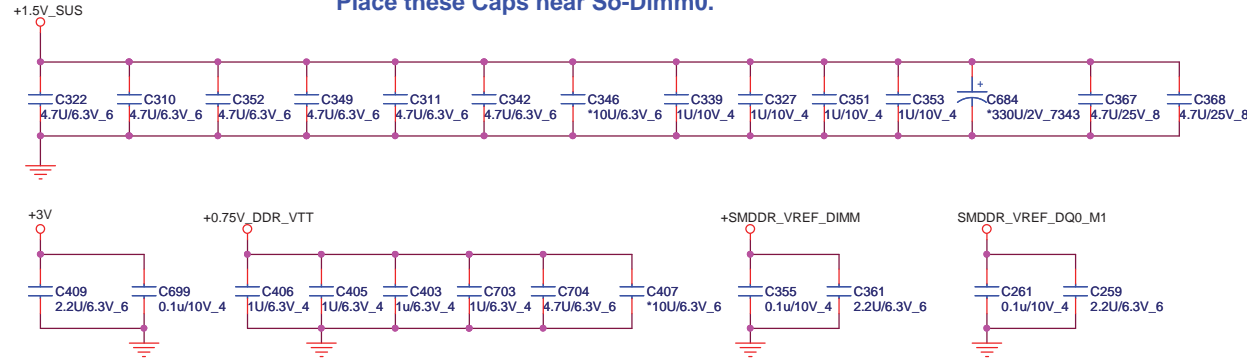
DDR STD (DDR)



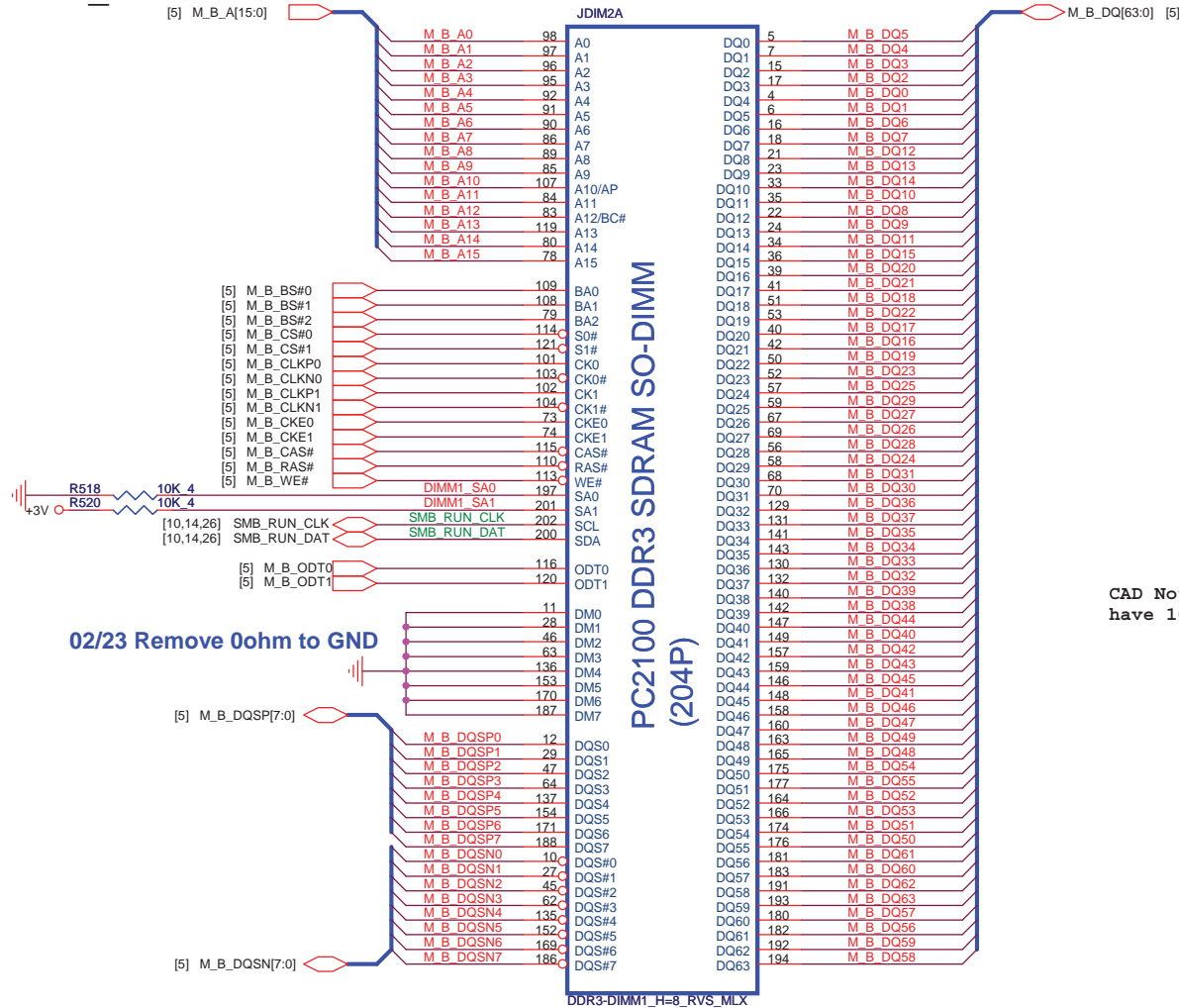
CAD Note: All VREF traces should have 10 mil trace width

02/23 Remove 0ohm to GND

Place these Caps near So-Dimm0.



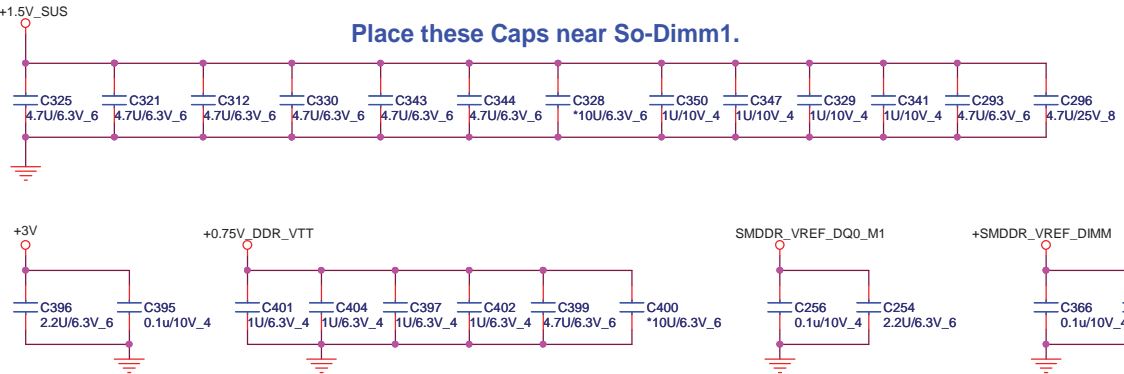
DDR_RVS (DDR)



CAD Note: All VREF traces should have 10 mil trace width

2.48A

02/23 Remove 0ohm to GND



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

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PROJECT : ZRJ

Size Document Number

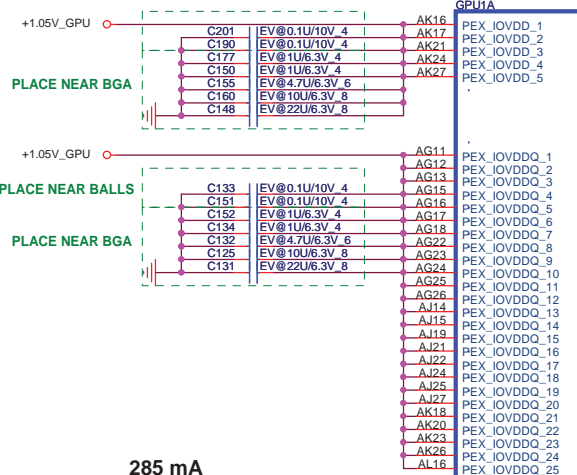
DDRIII SO-DIMM-1

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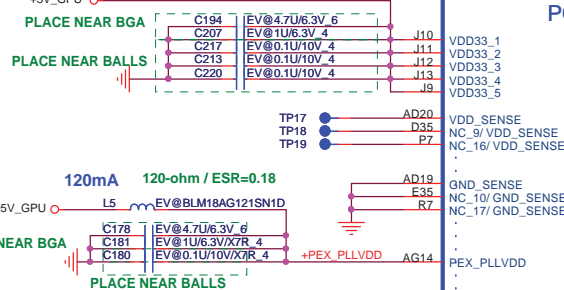
Rev 1A

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

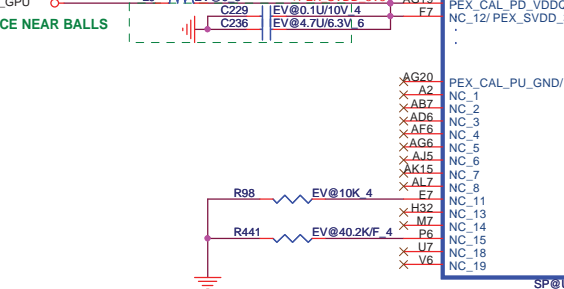
2200mA
PLACE NEAR BALLS



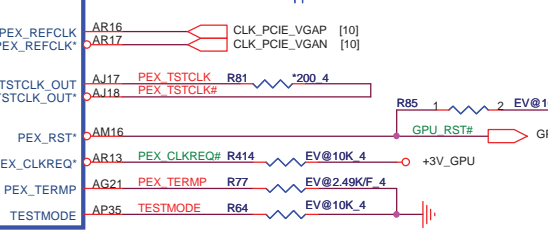
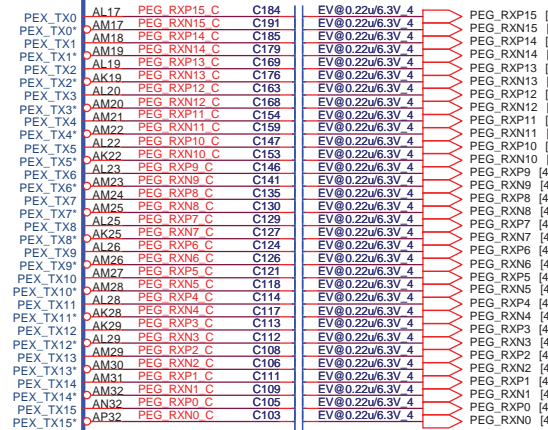
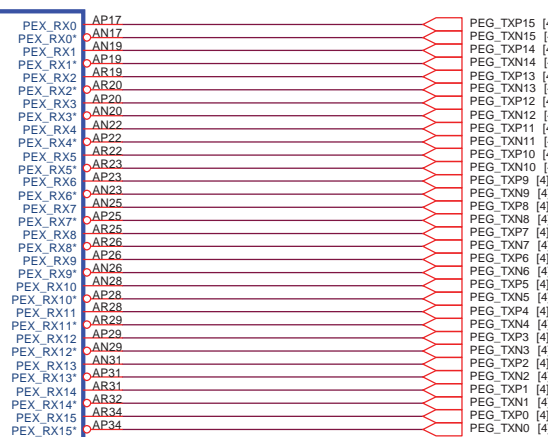
+3V_GPU 285 mA



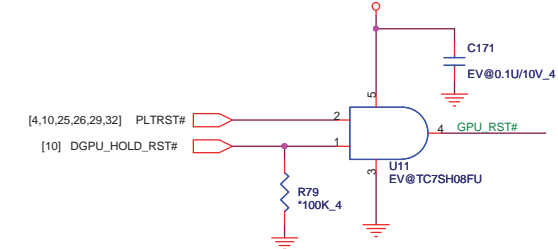
+3V_GPU 120mA



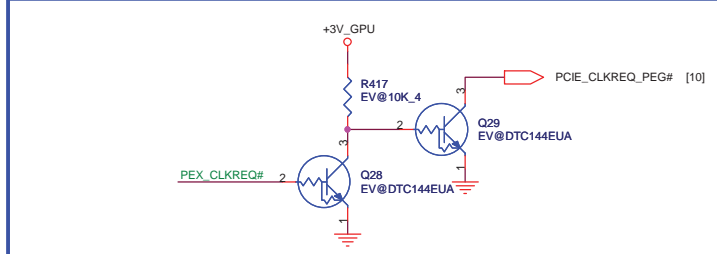
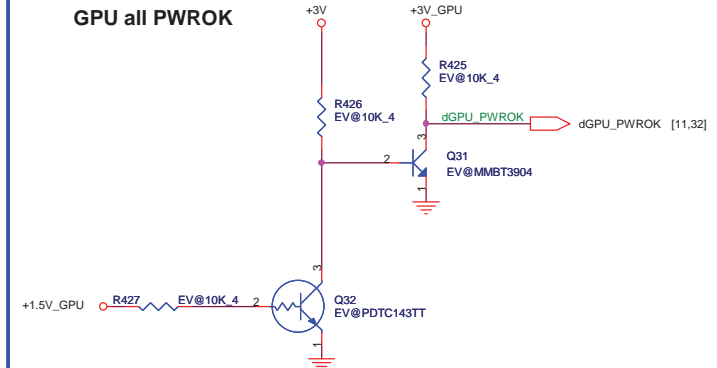
PCI EXPRESS



GPU_RST#



GPU all PWROK

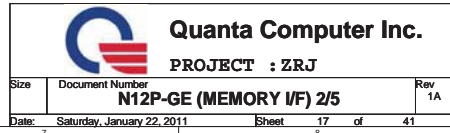


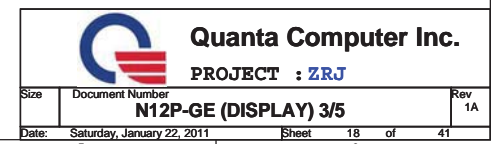
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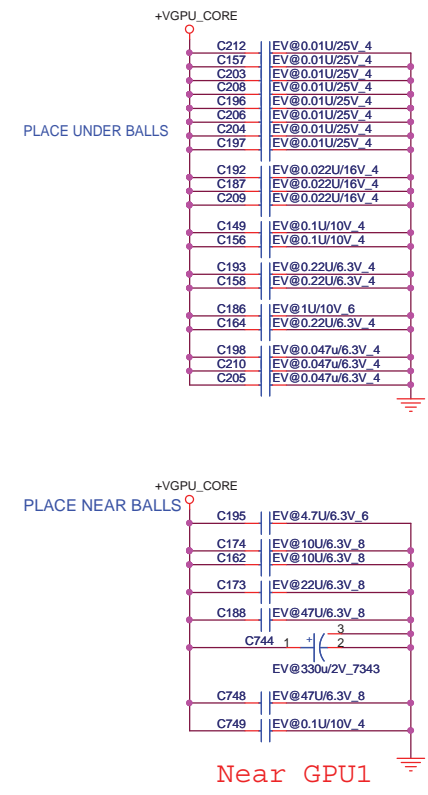
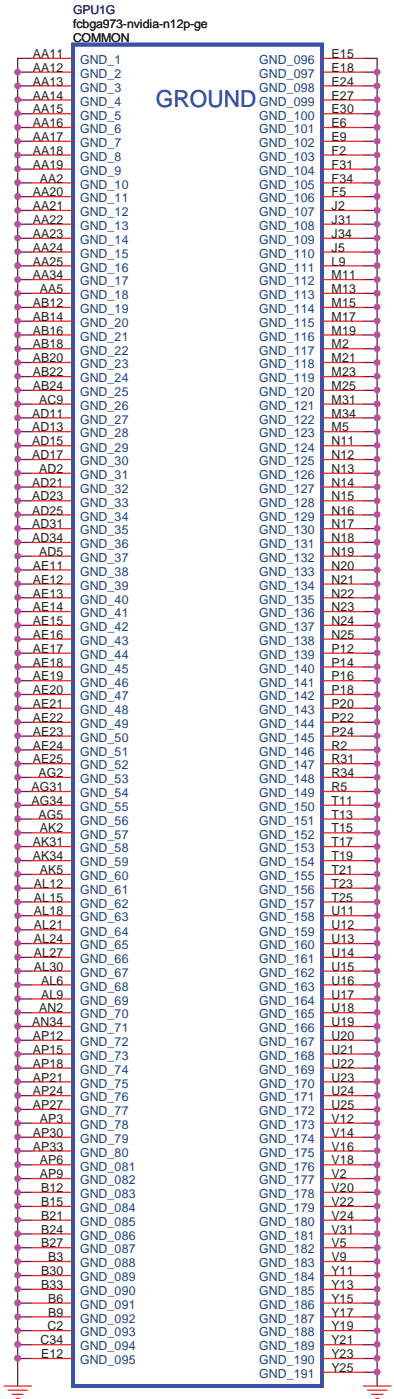
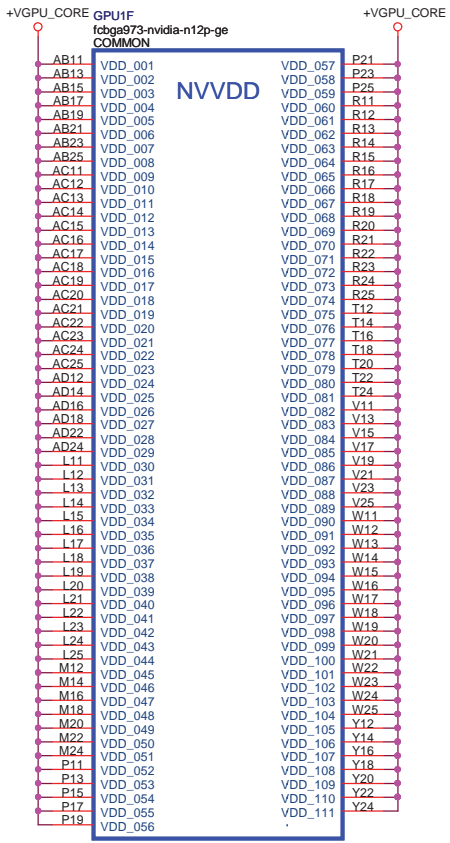
PROJECT : ZRJ

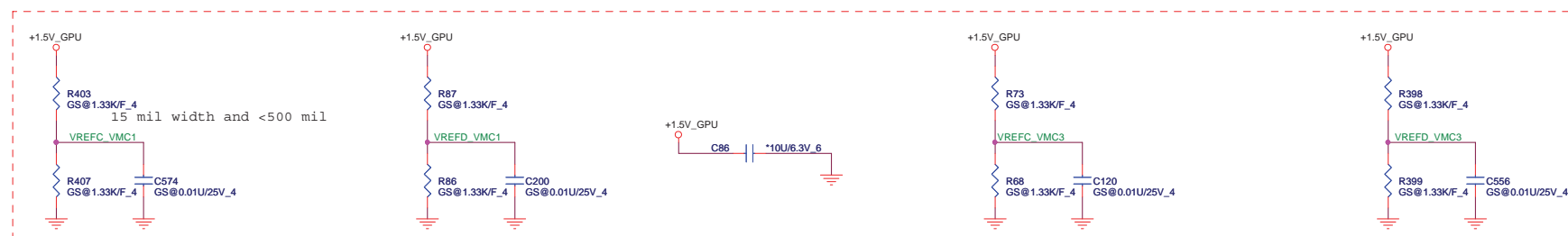
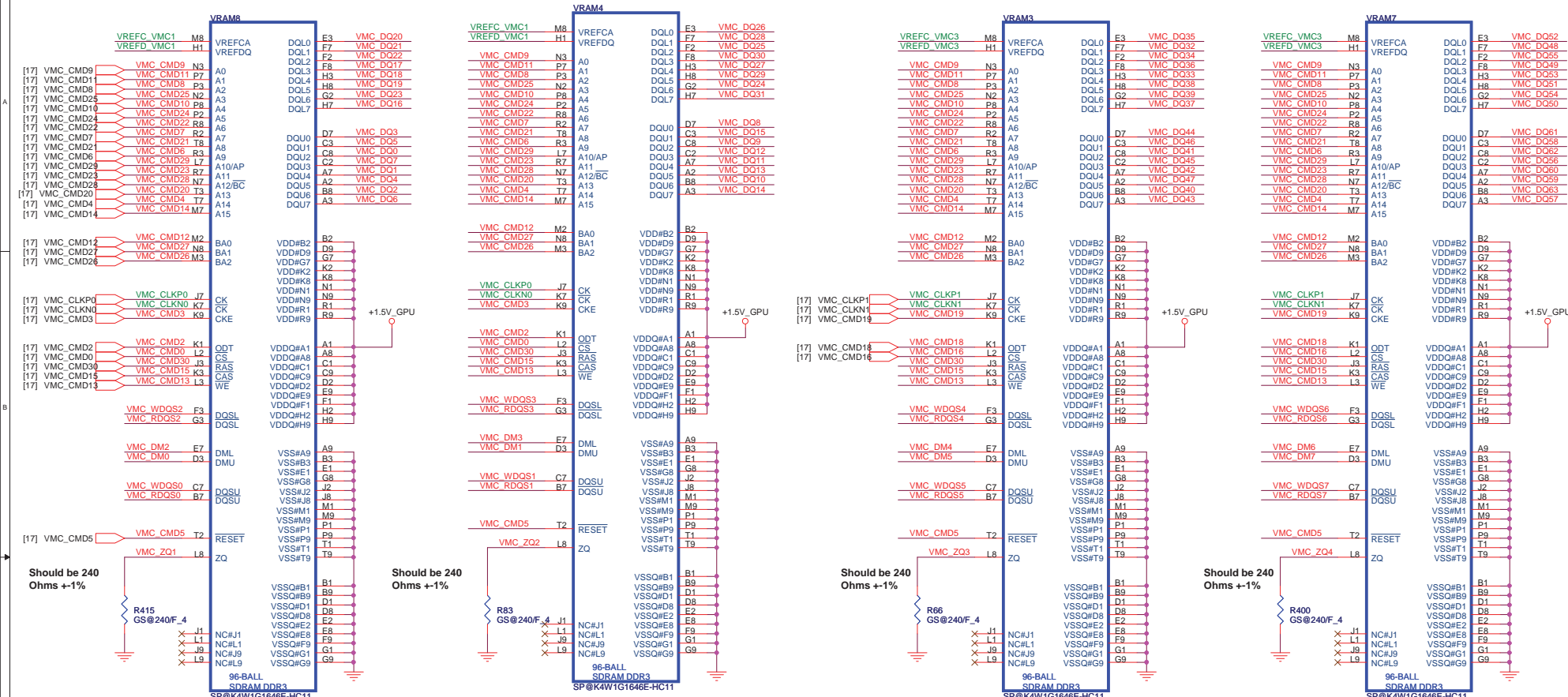
N12P-GE (PCIE I/F) 1/5

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1A		
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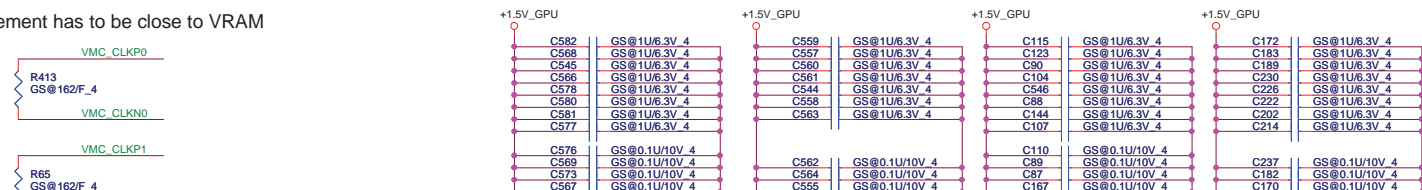


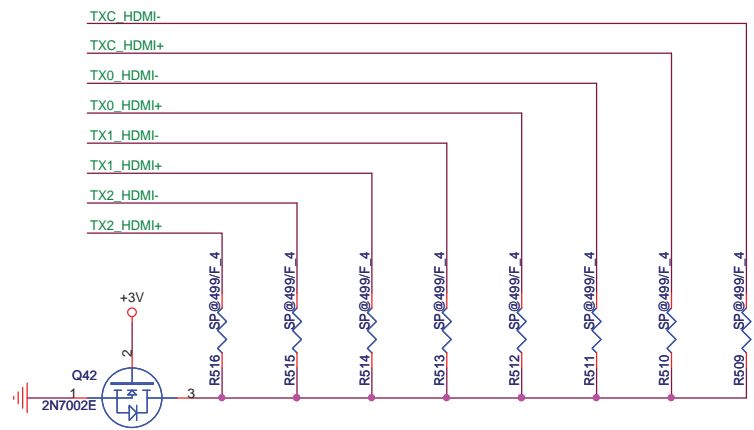






Placement has to be close to VRAM

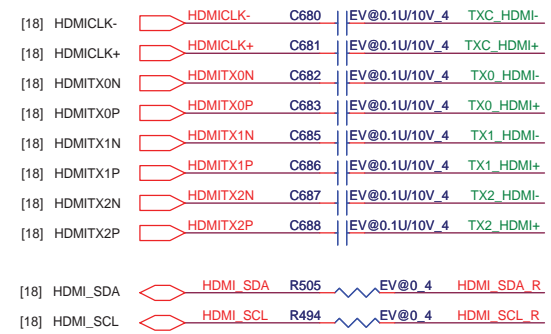




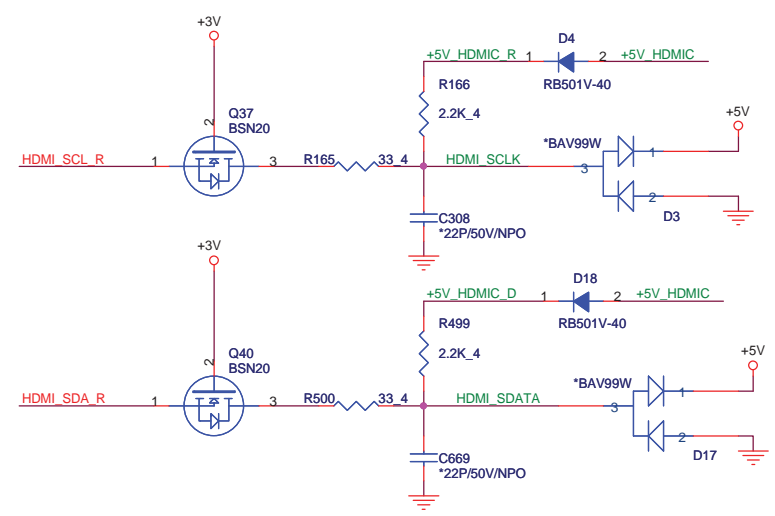
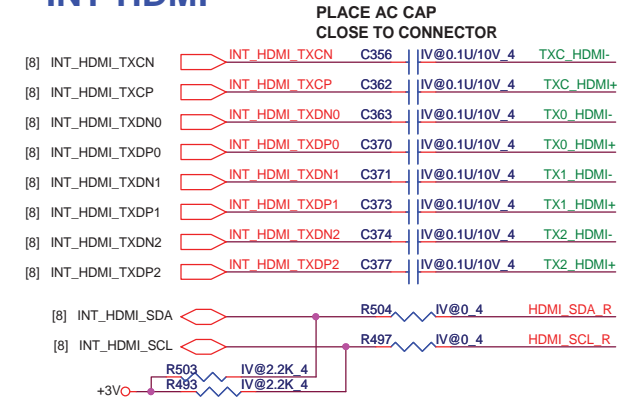
	EV@	IV@
SP@	500 ohm	680 ohm

PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

EXT-HDMI

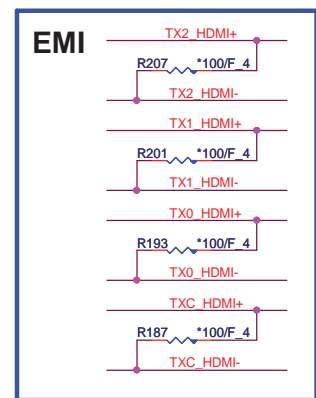


INT-HDMI

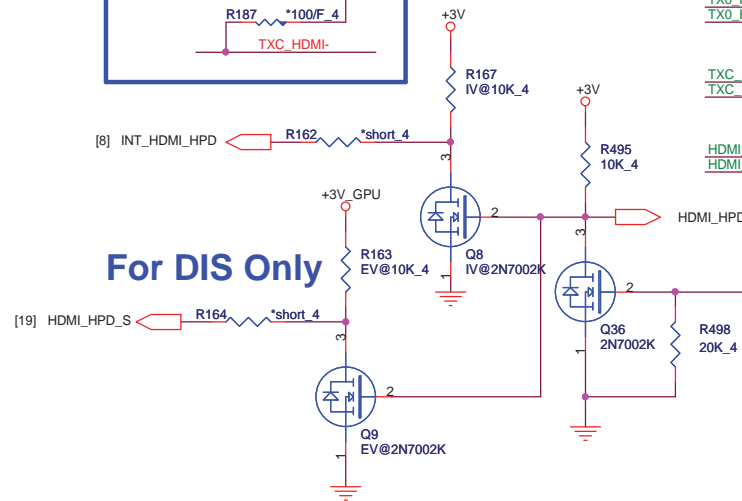


For UMA / Optimus HDMI function

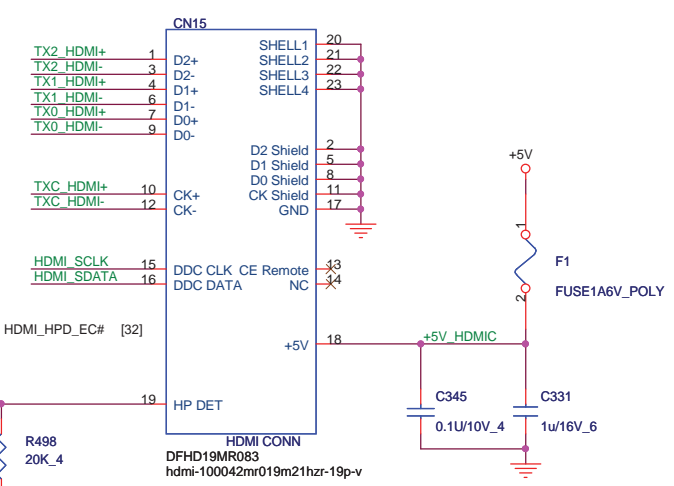
EMI



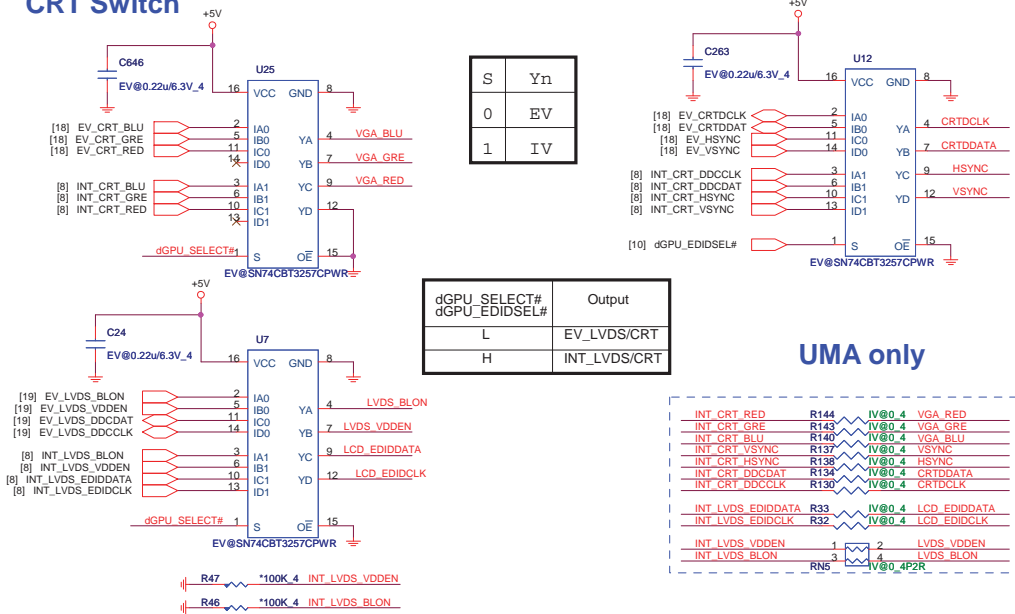
For DIS Only



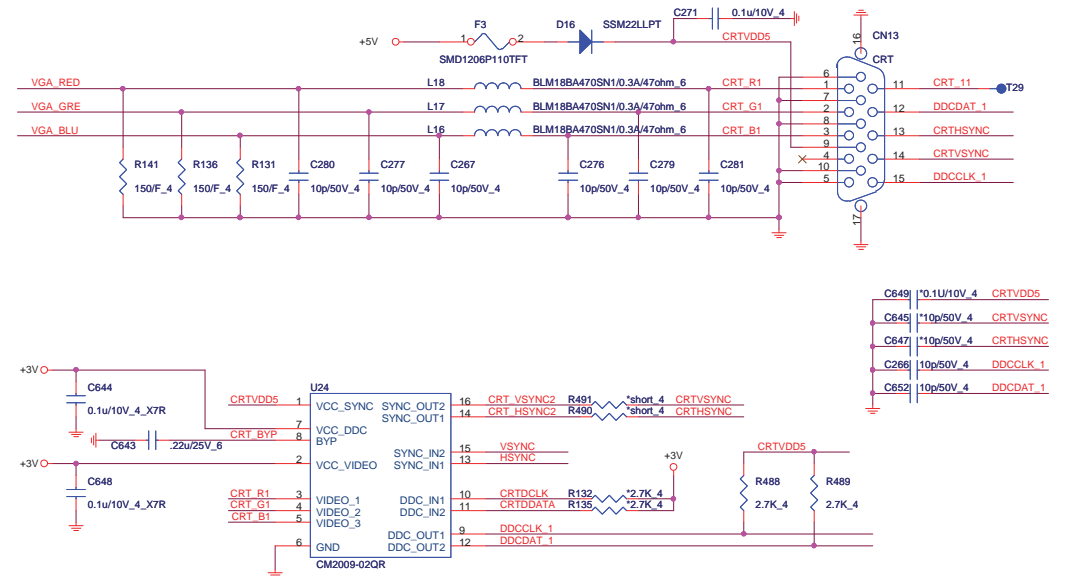
HDMI CONN



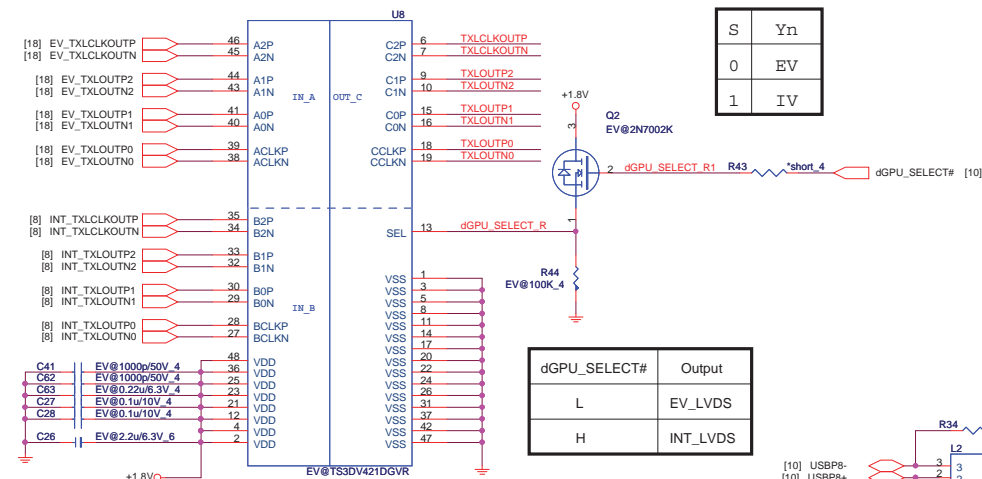
CRT Switch



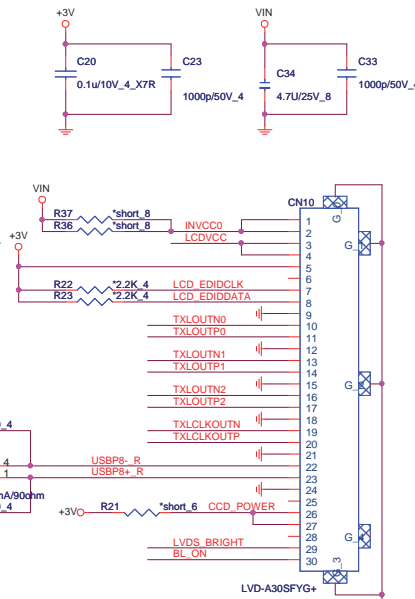
CRT



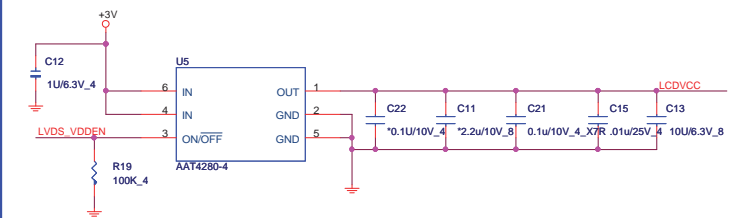
LVDS Switch



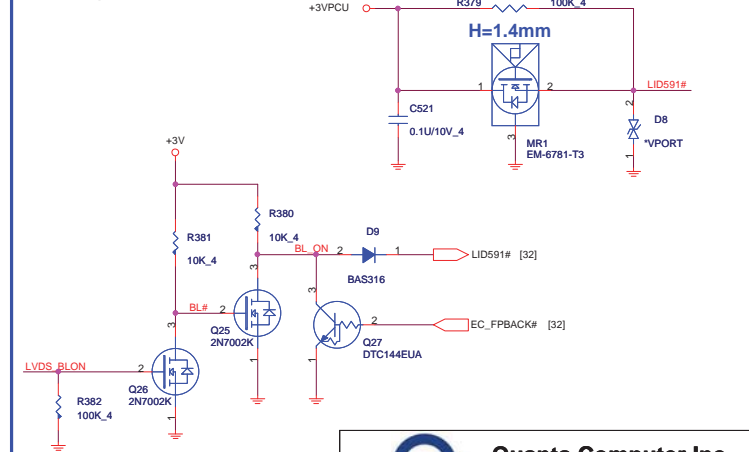
LVDS



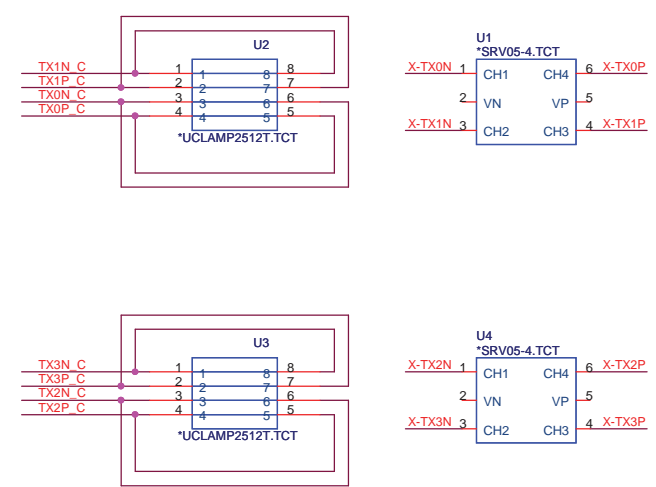
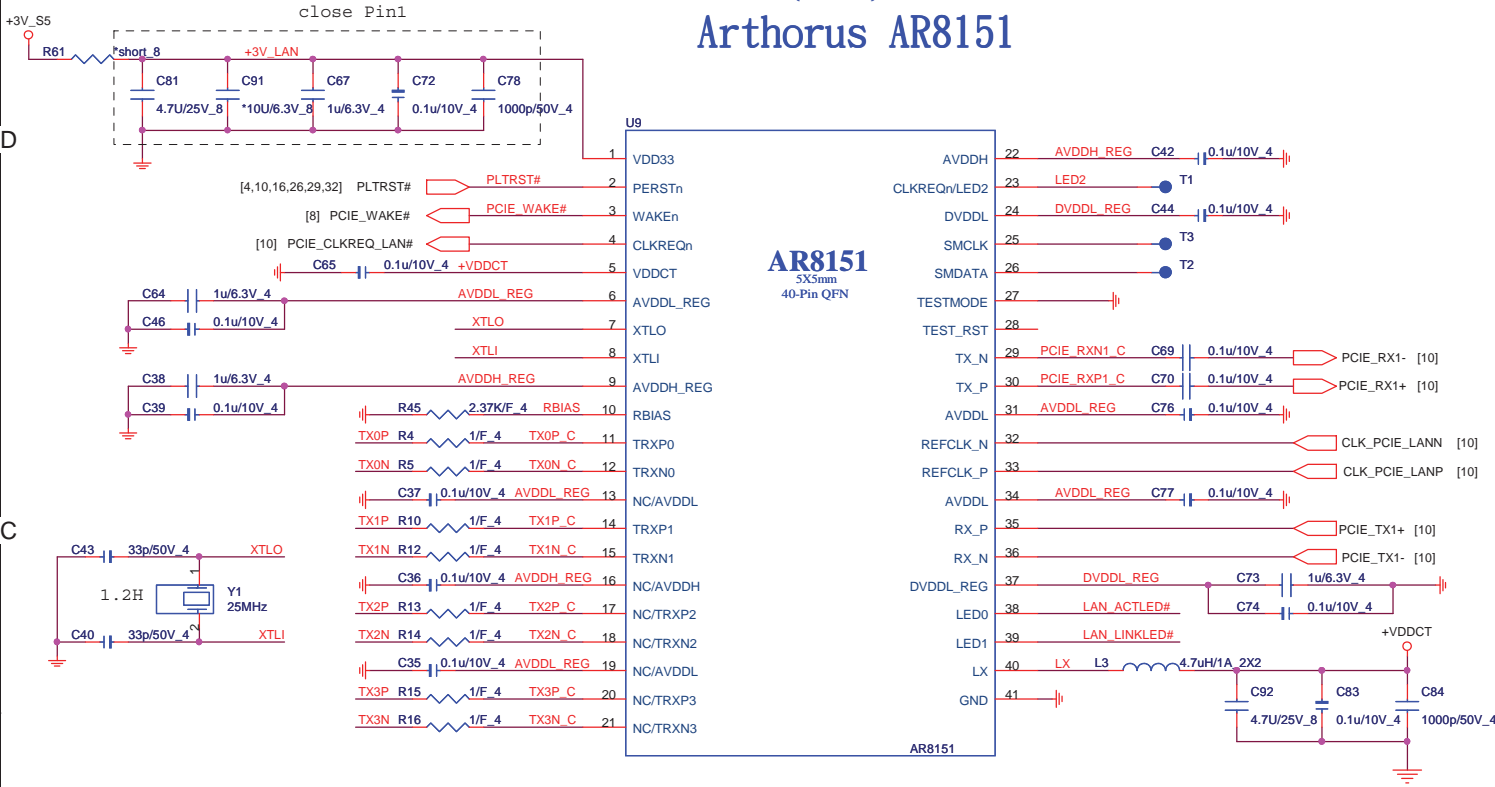
LCD Power



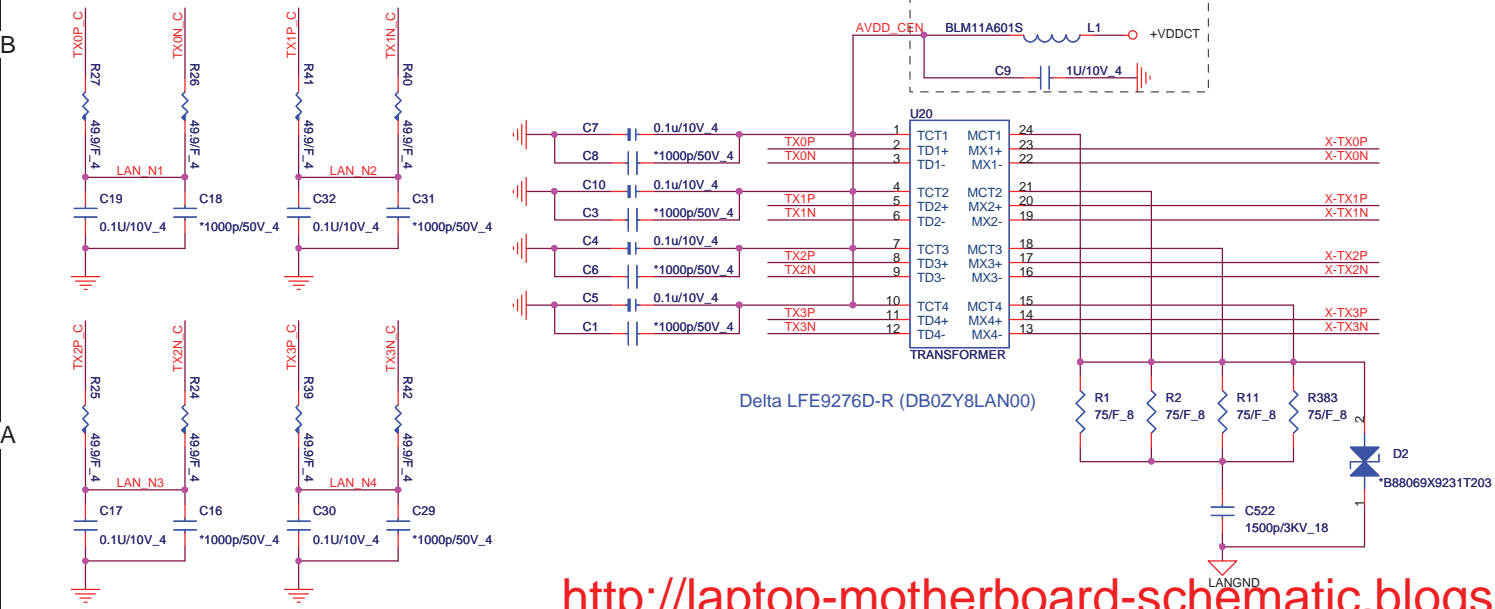
Backlight Control



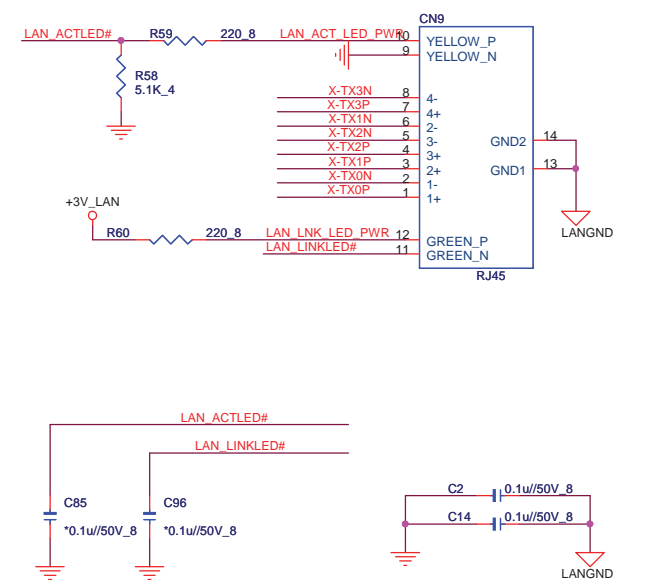
LAN (LAN) Arthorus AR8151



TRANSFORMER(LAN)

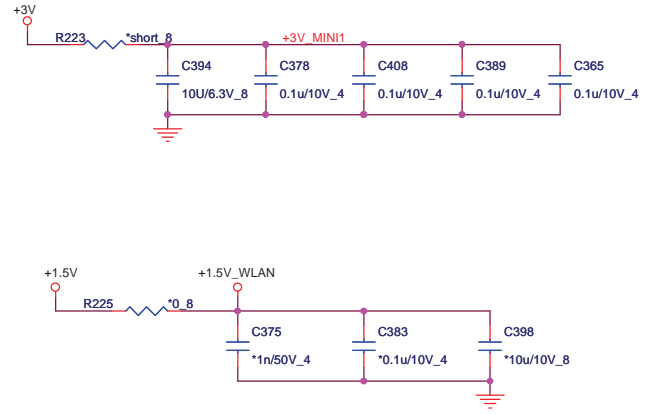
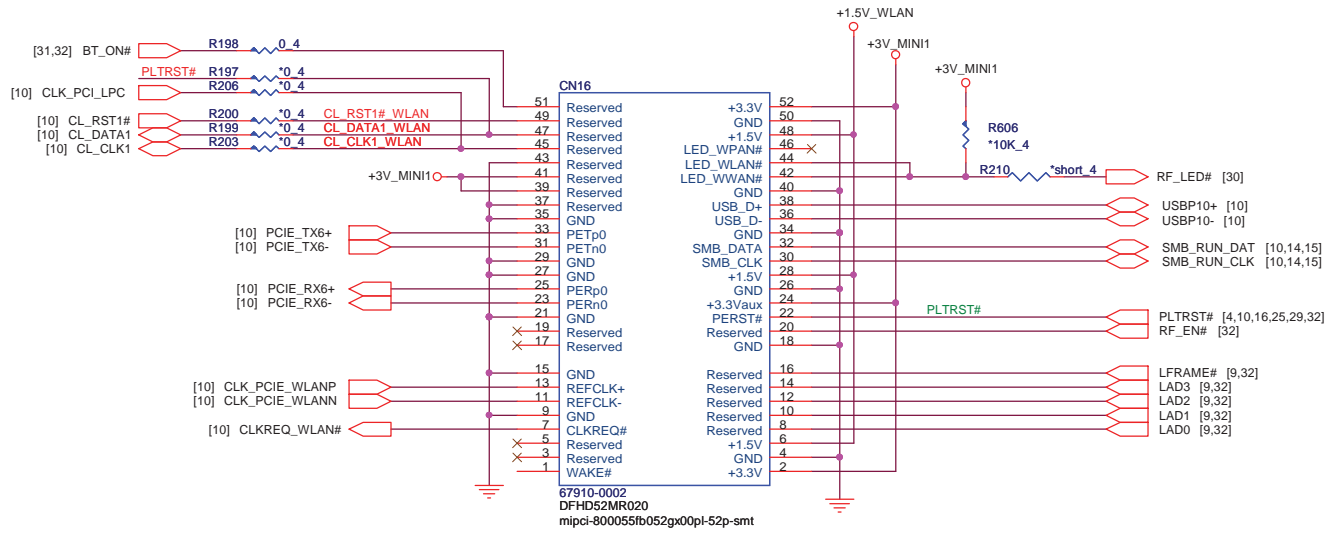


RJ45(LAN)

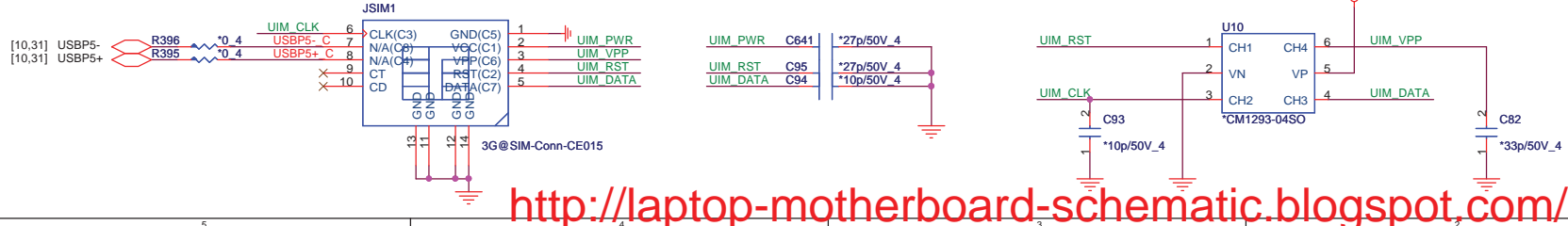
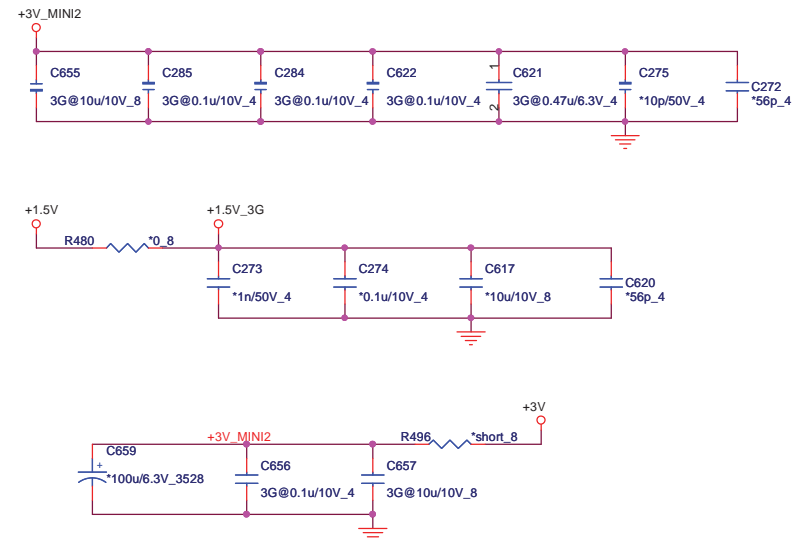
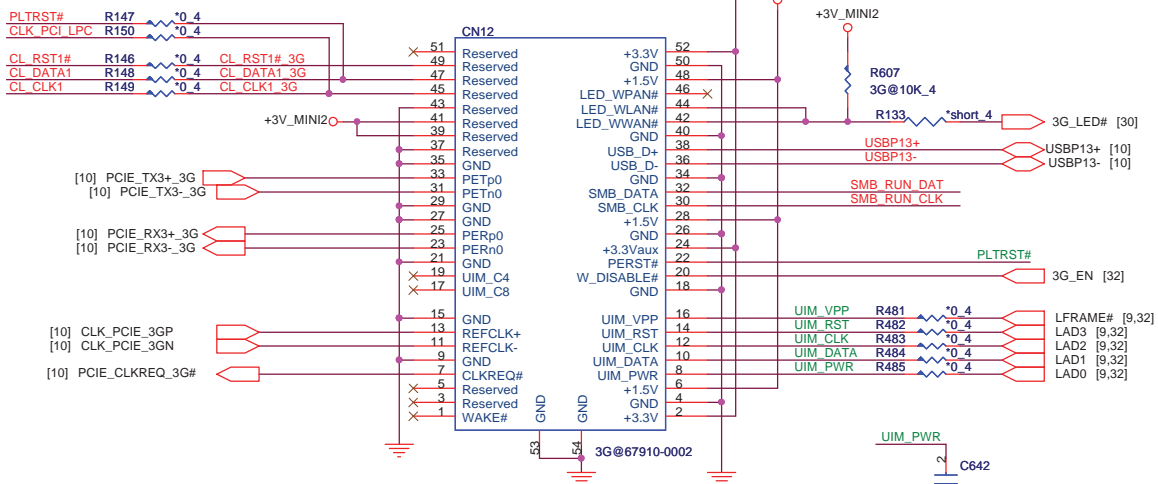



MINI CARD (WLAN) H=7

26



Mini Card2-3G (MNC) H=9



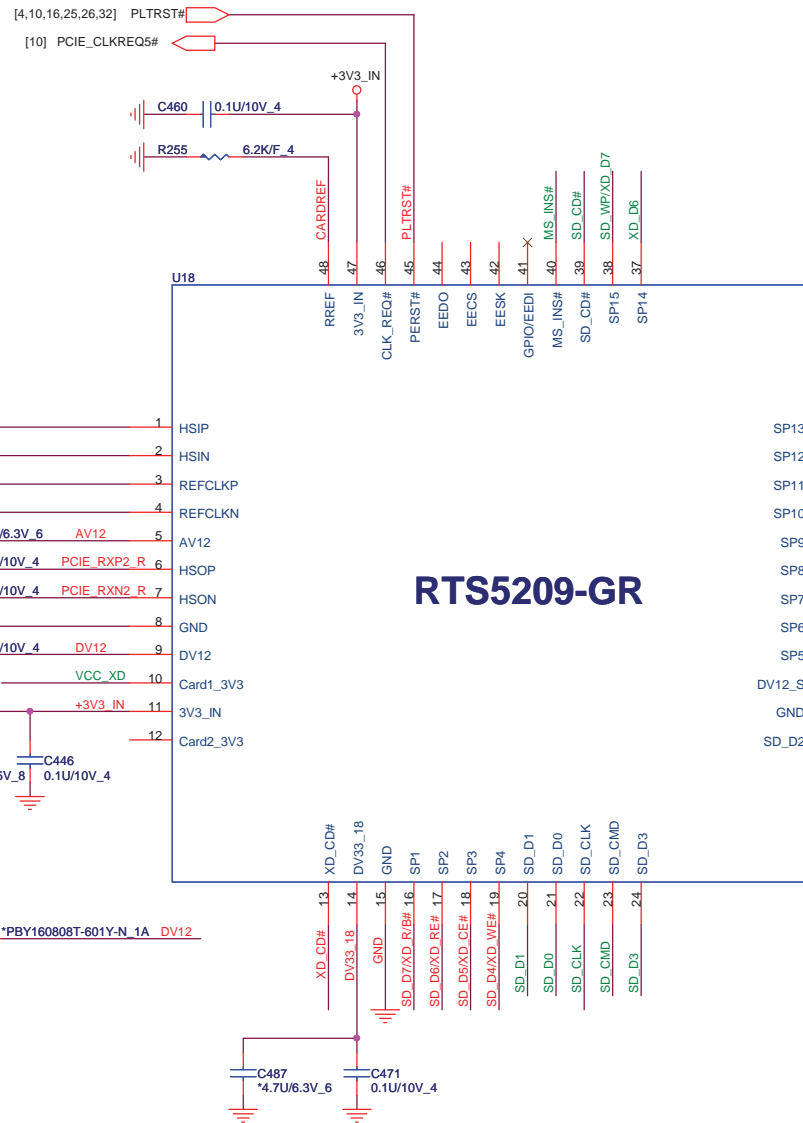


Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	MINI CARD(WLAN/3G)	1A
Date:	Saturday, January 22, 2011	Sheet 26 of 41

Card reader controller

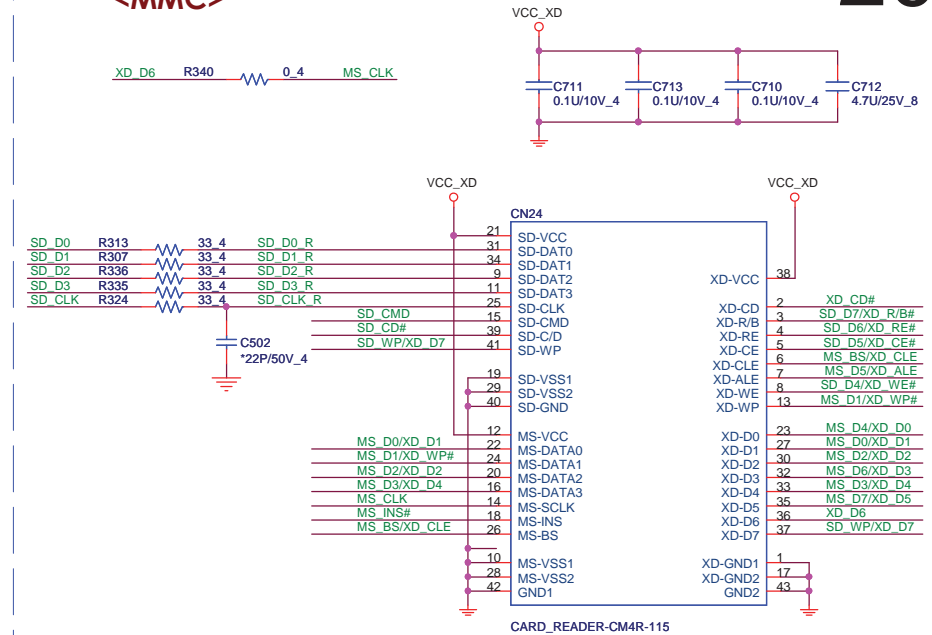
<MMC>




RTS5209-GR

5 IN 1 Card reader CONN

<MMC>



20

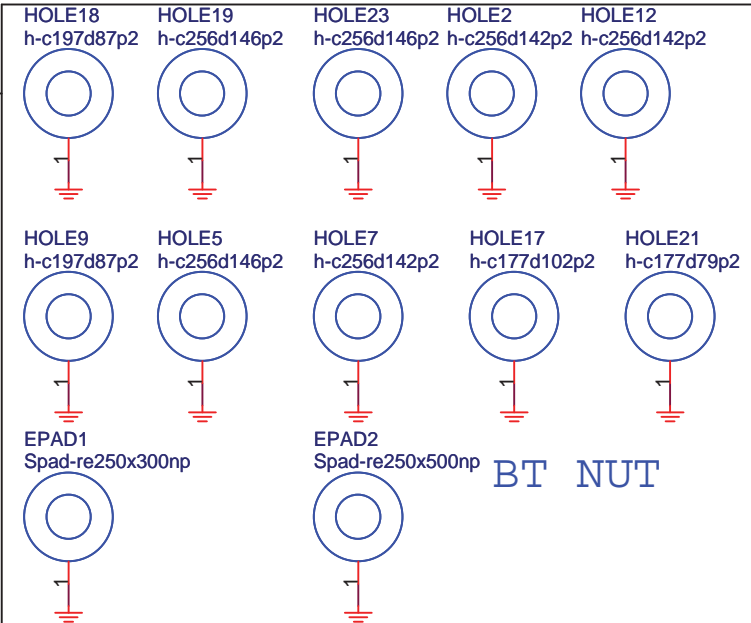
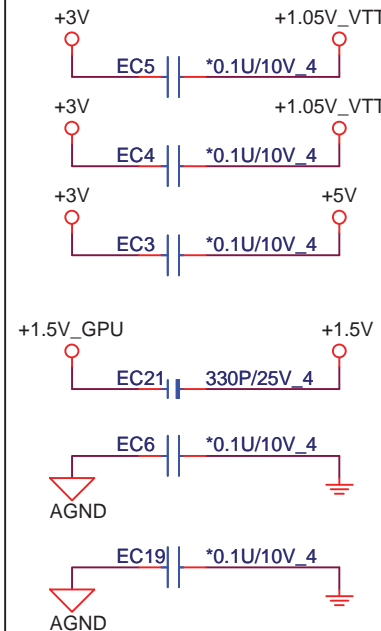
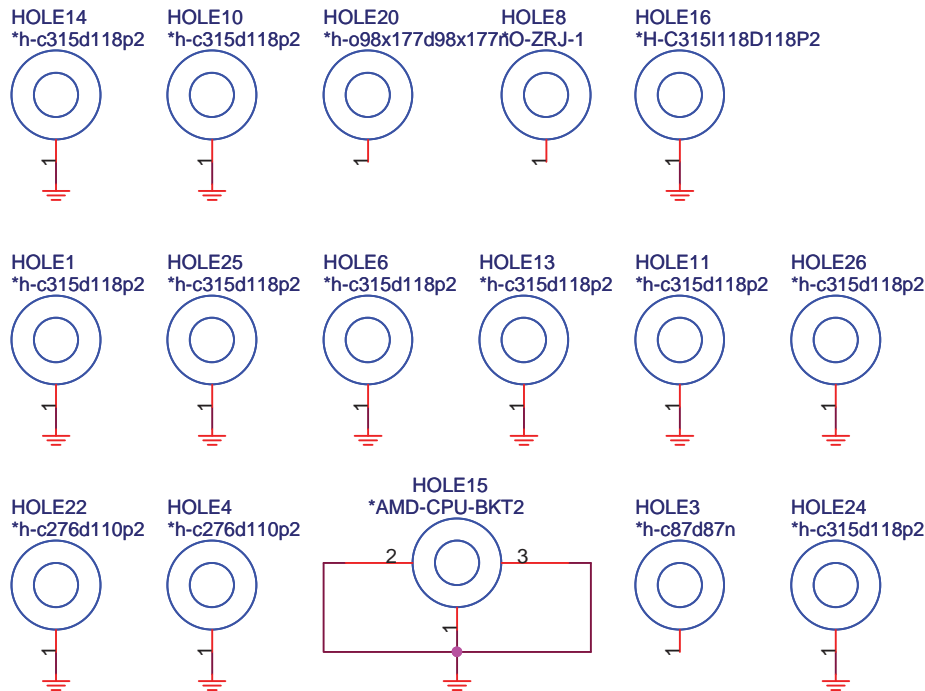
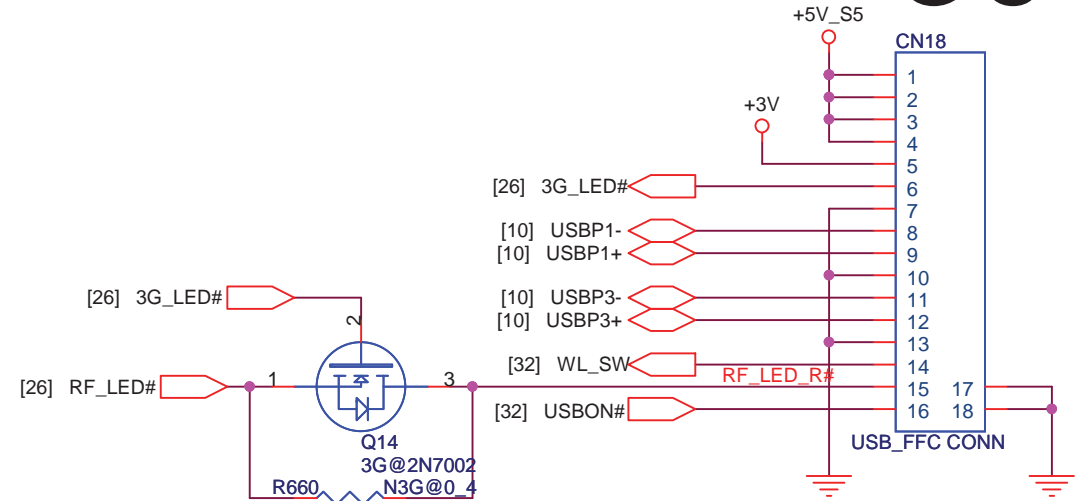
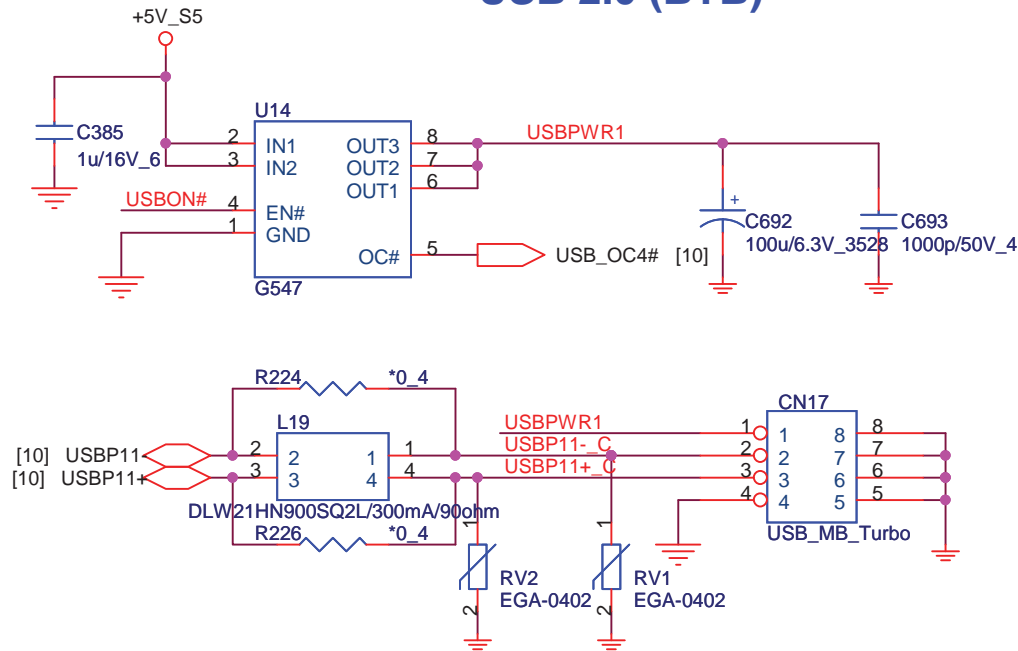


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		3G
Date	Saturday, January 22, 2011	Sheet 29 of 41

USB 2.0 (BTB)

30

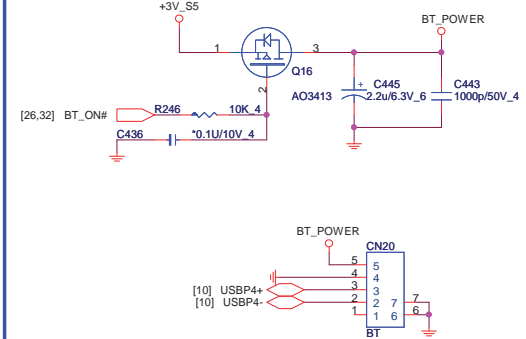


Quanta Computer Inc.

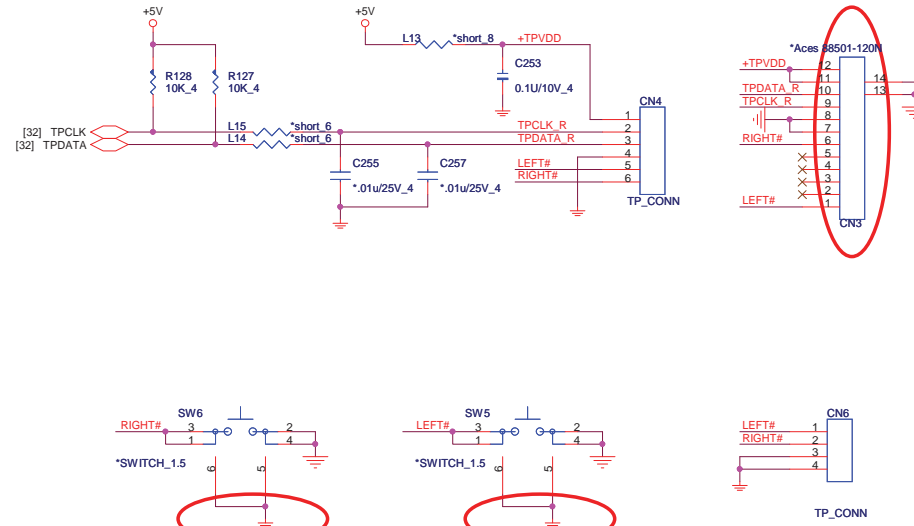
PROJECT : ZRJ

Size	Document Number	Rev
	USB2.0 Board (Dual Way)	1A
Date:	Monday, January 24, 2011	Sheet 30 of 41

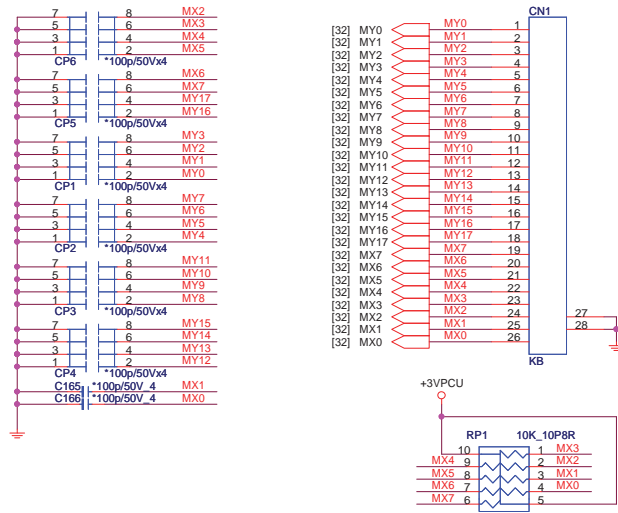
Bluetooth (BTM)



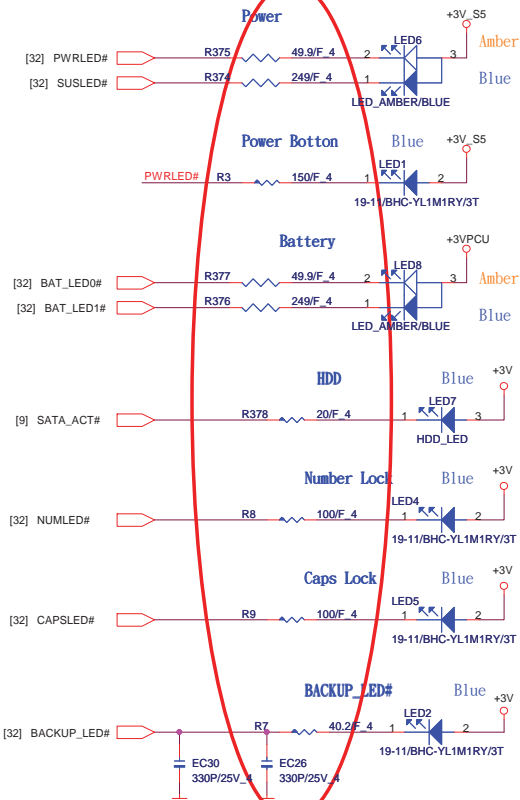
TouchPad (TPD)



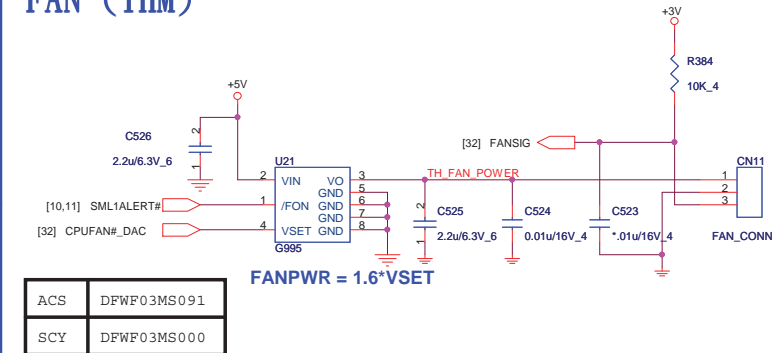
Keyboard (KBC)



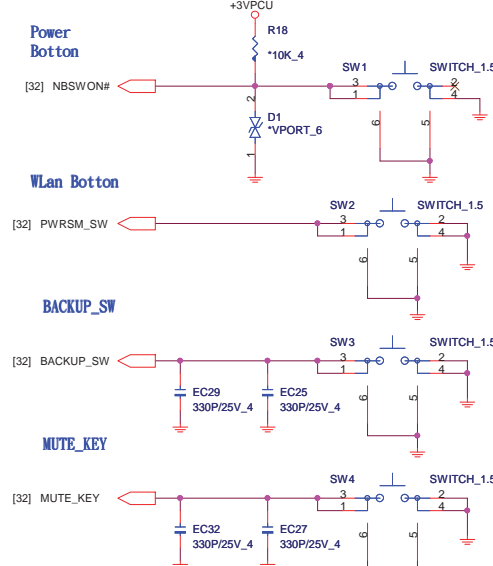
LEDs (UIF)



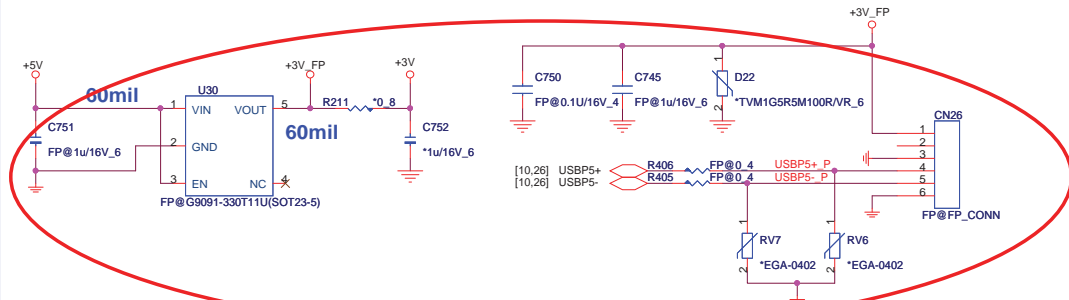
FAN (THM)

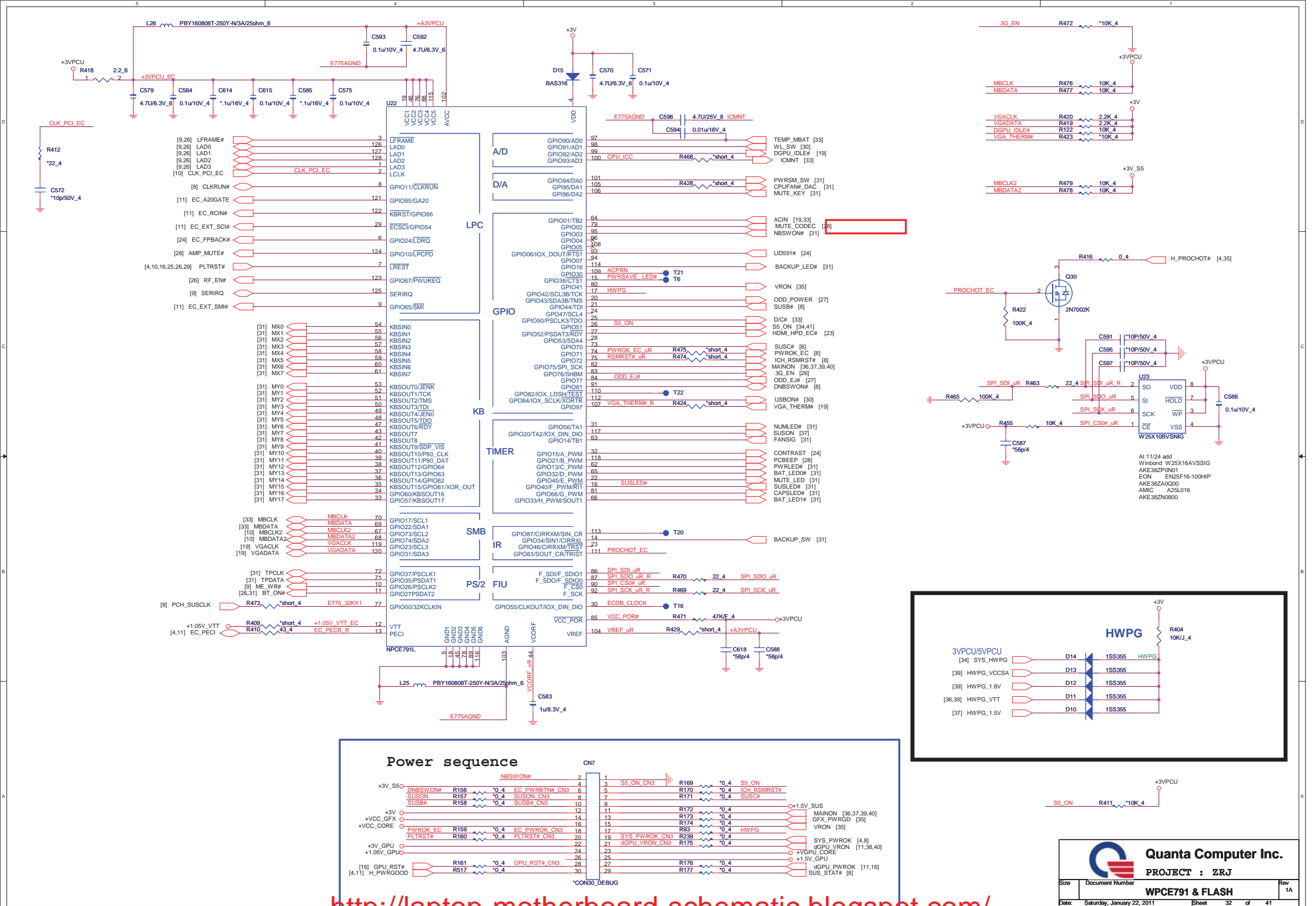


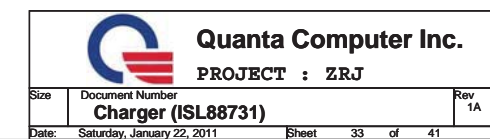
Buttons (UIF)

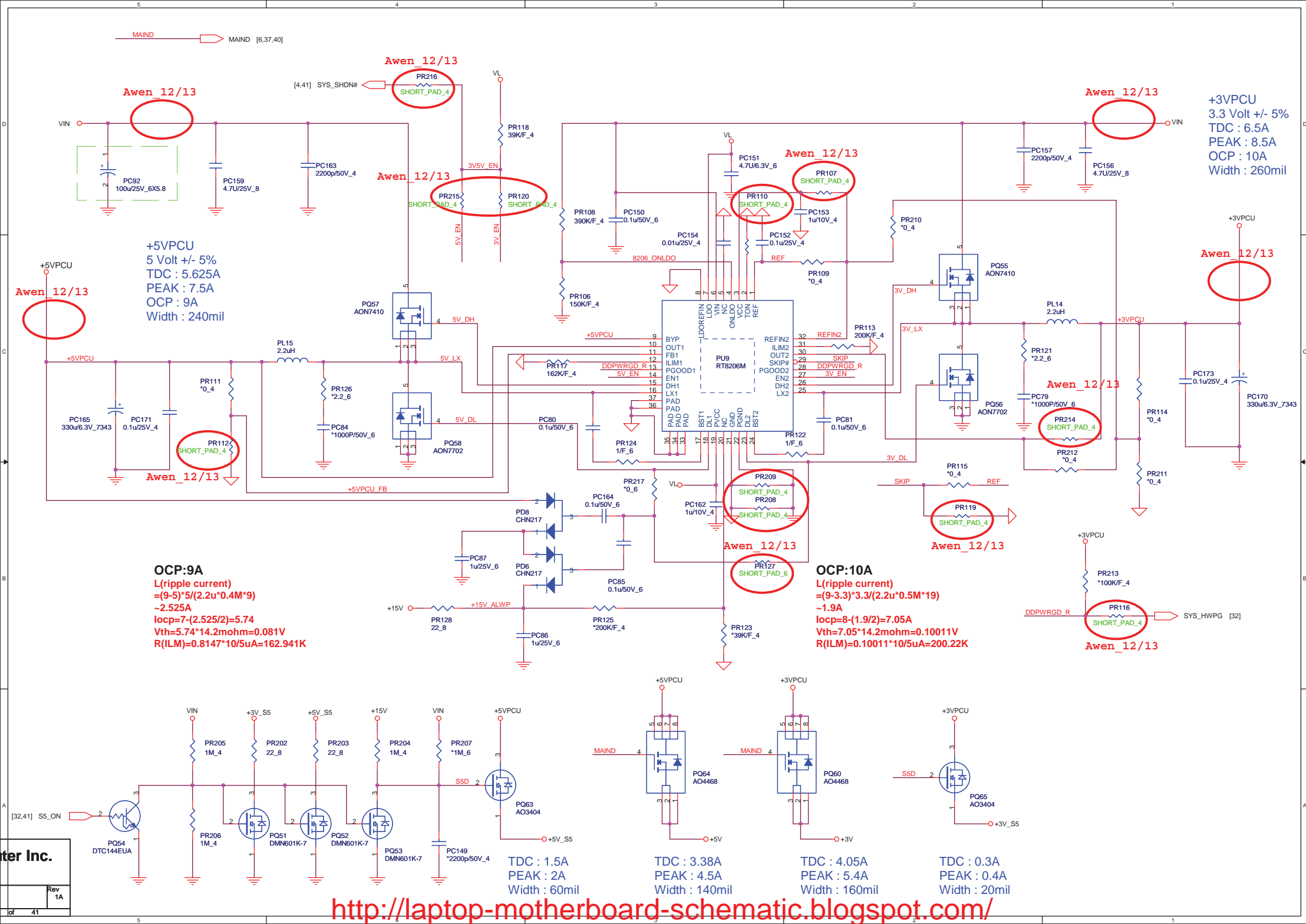


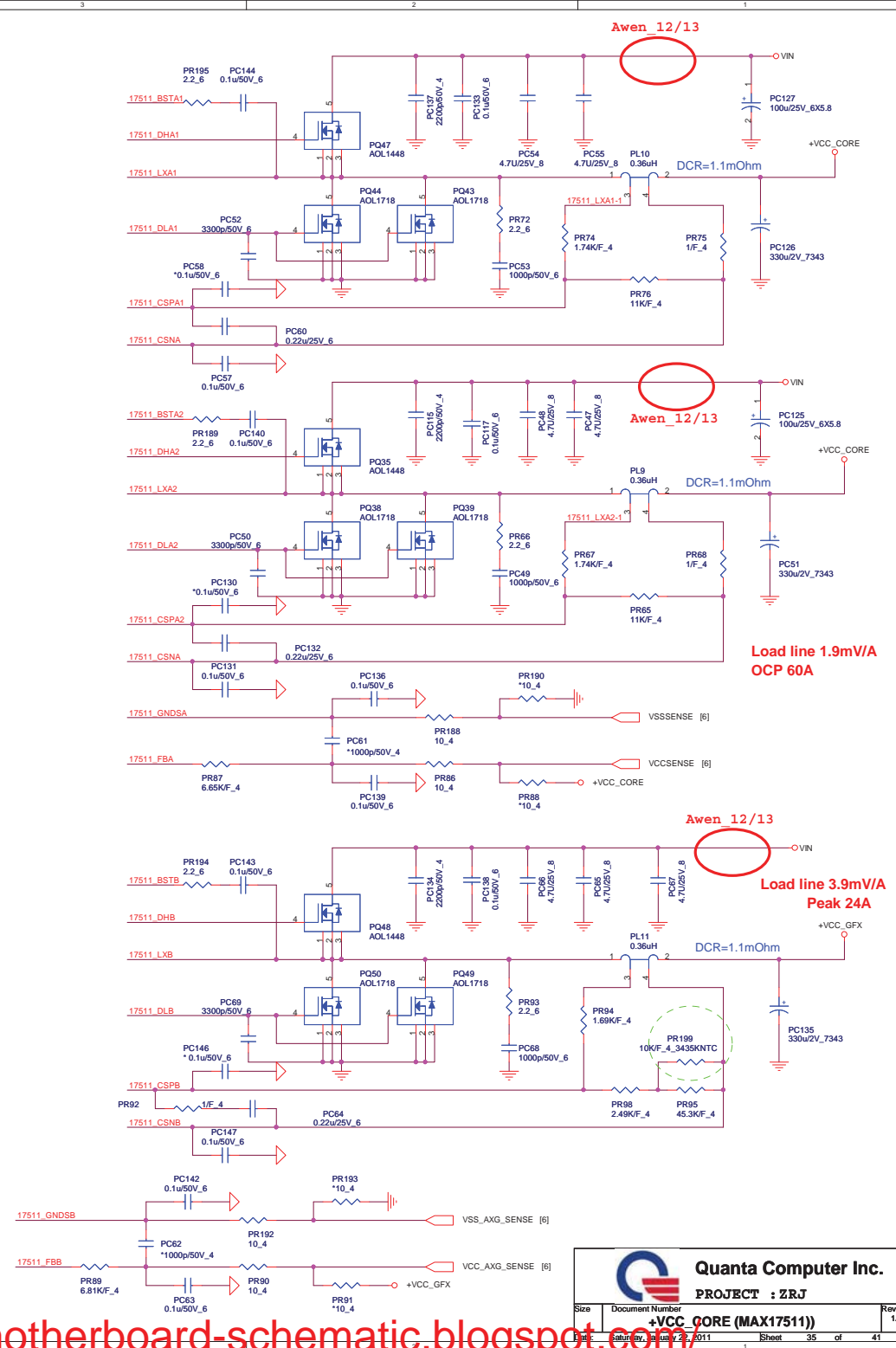
Finger-Printer CONN.



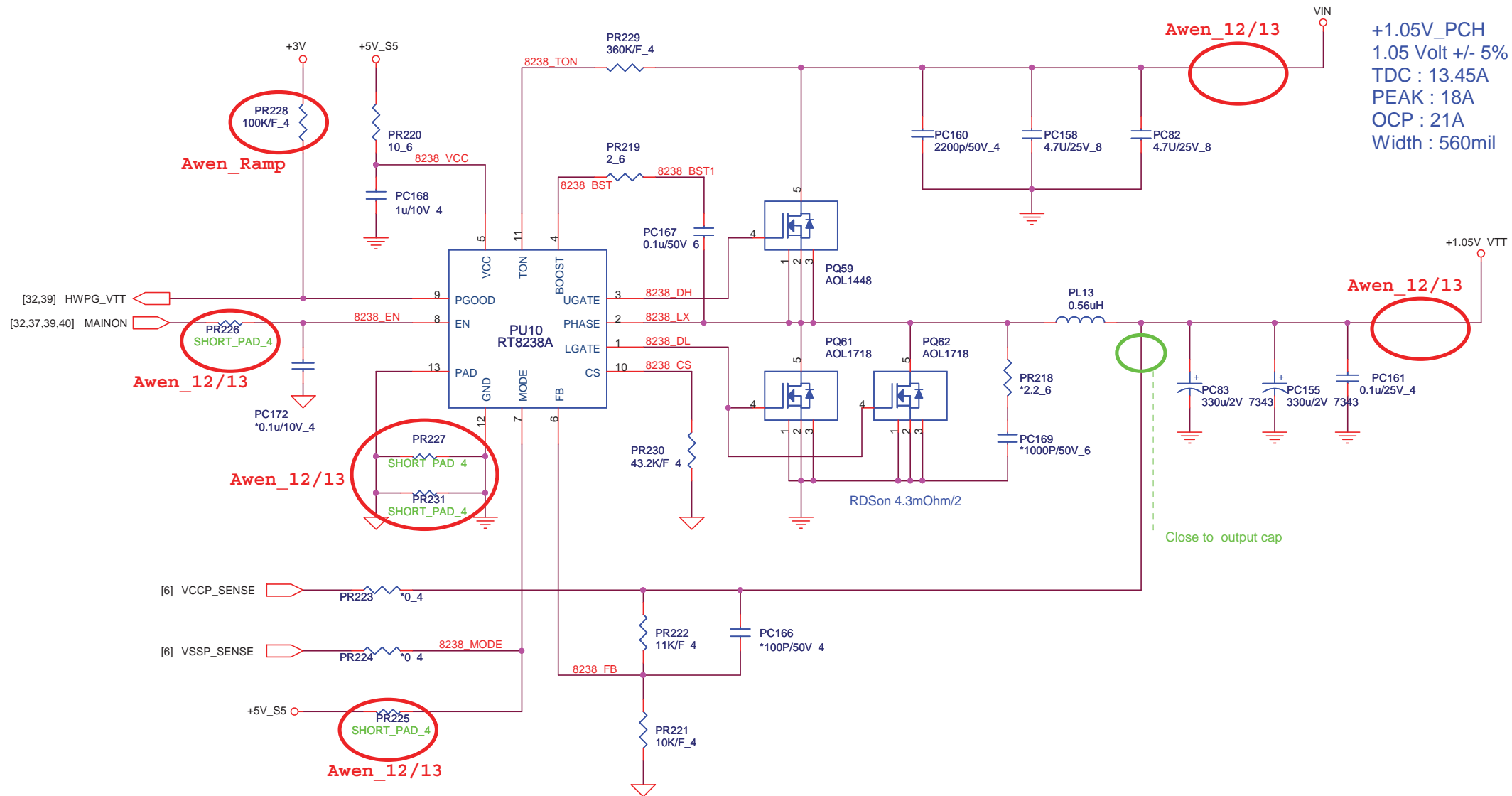






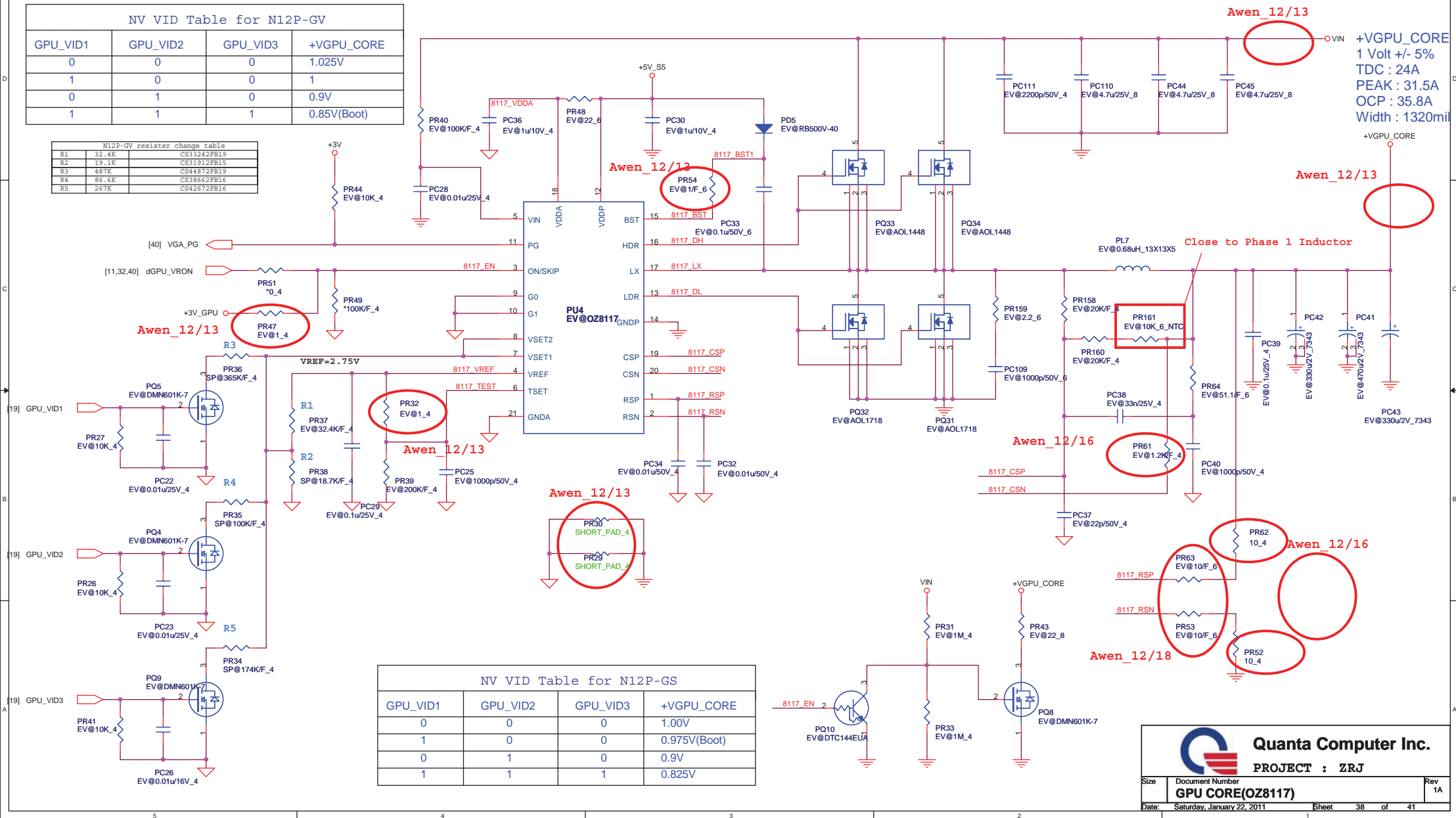


	UMA (iV@) / Muxless (MS@)	External VGA (EV@)
PR196	NC	Populated
PR85	100K/F_4 (CS41002FB28)	200K/F_4 (CS42002FB12)
PR82	130K/F_4 (CS41302FB00)	NC
PR184	158K/F_4 (CS41582FB14)	NC
PR182	5.62K/F_4 (CS25622FB18)	1K/F_4 (CS21002FB24)
PR99	Populated	NC
PR198	Populated	NC



NV VID Table for N12P-GV			
GPU_VID1	GPU_VID2	GPU_VID3	+VGPU_CORE
0	0	0	1.025V
1	0	0	1
0	1	0	0.9V
1	1	1	0.85V(Boot)

N12P-GV resistor change table			
R1	32.4K	CS33242PB19	
R2	19.1K	CS31912PB15	
R3	487K	CS44872PB19	
R4	86.6K	CS38662PB16	
R5	267K	CS42672PB16	

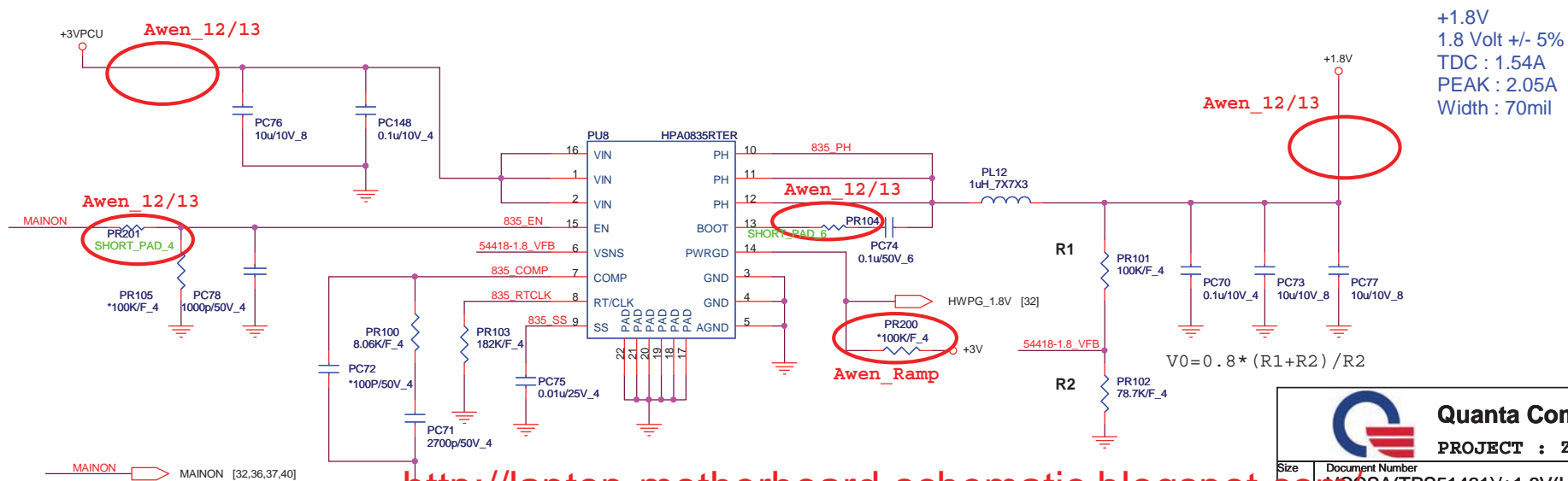
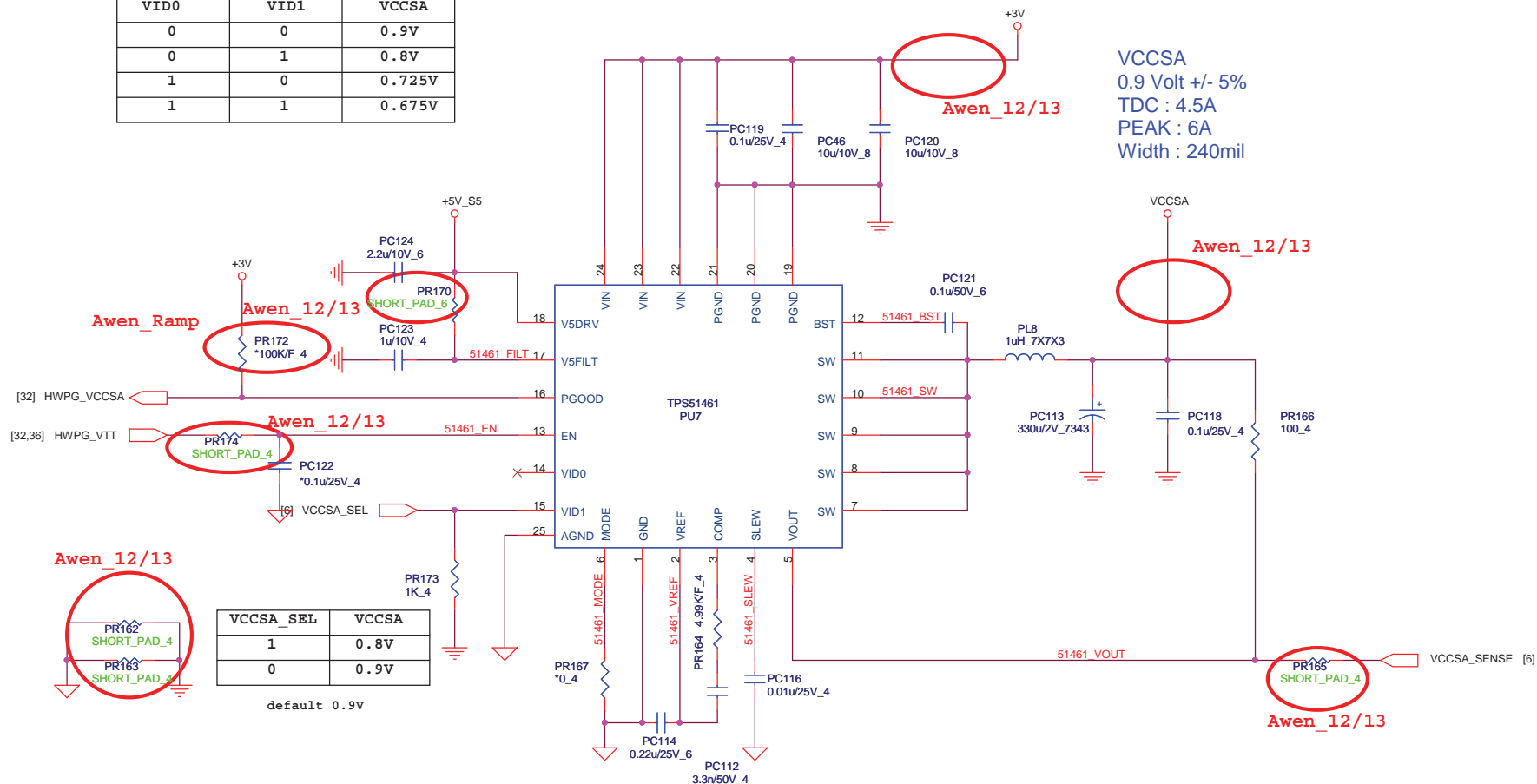


NV VID Table for N12P-GS			
GPU_VID1	GPU_VID2	GPU_VID3	+VGPU_CORE
0	0	0	1.00V
1	0	0	0.975V(Boot)
0	1	0	0.9V
1	1	1	0.825V

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Size	Document Number	Rev
	GPU CORE(OZ8117)	1A
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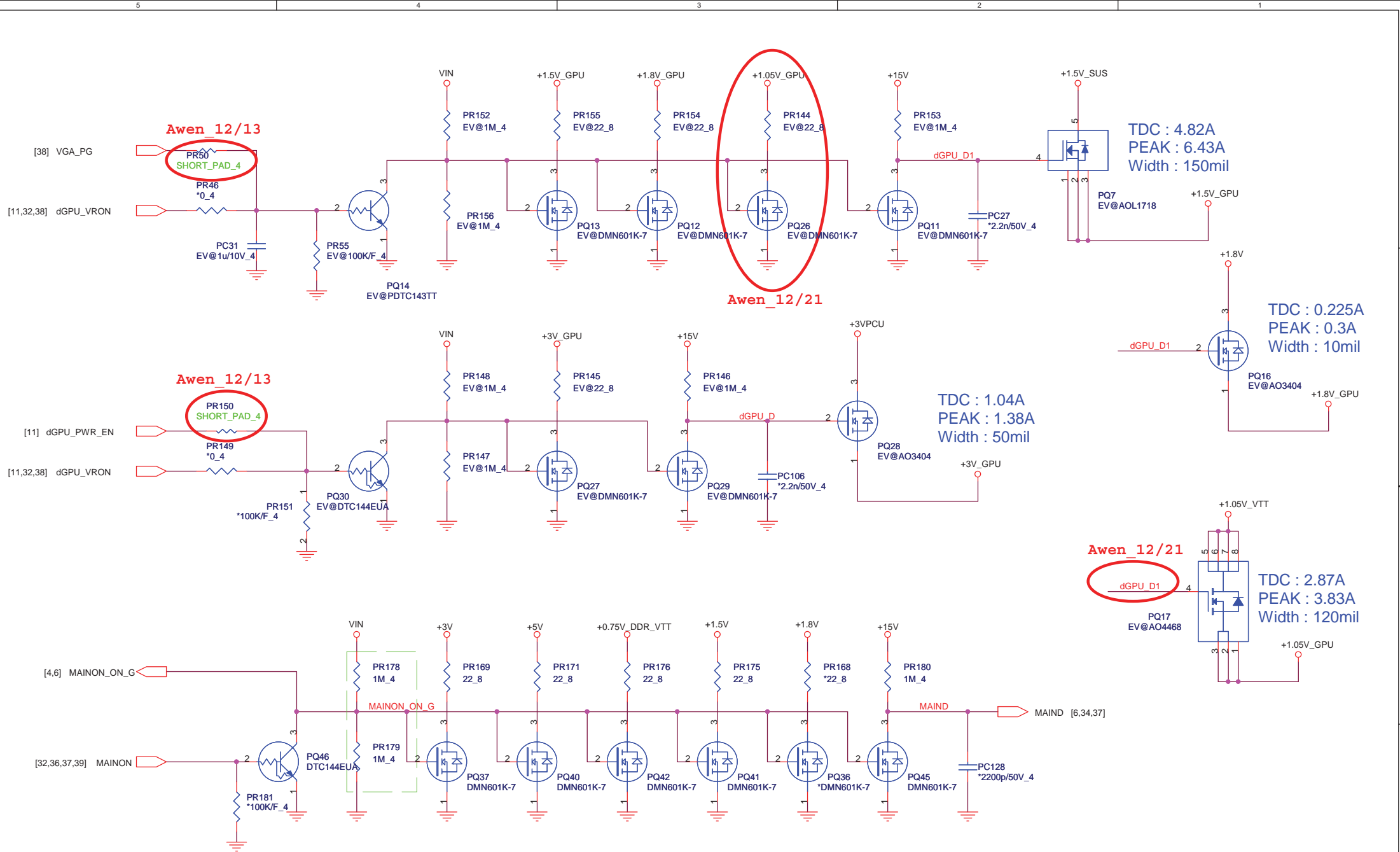
VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



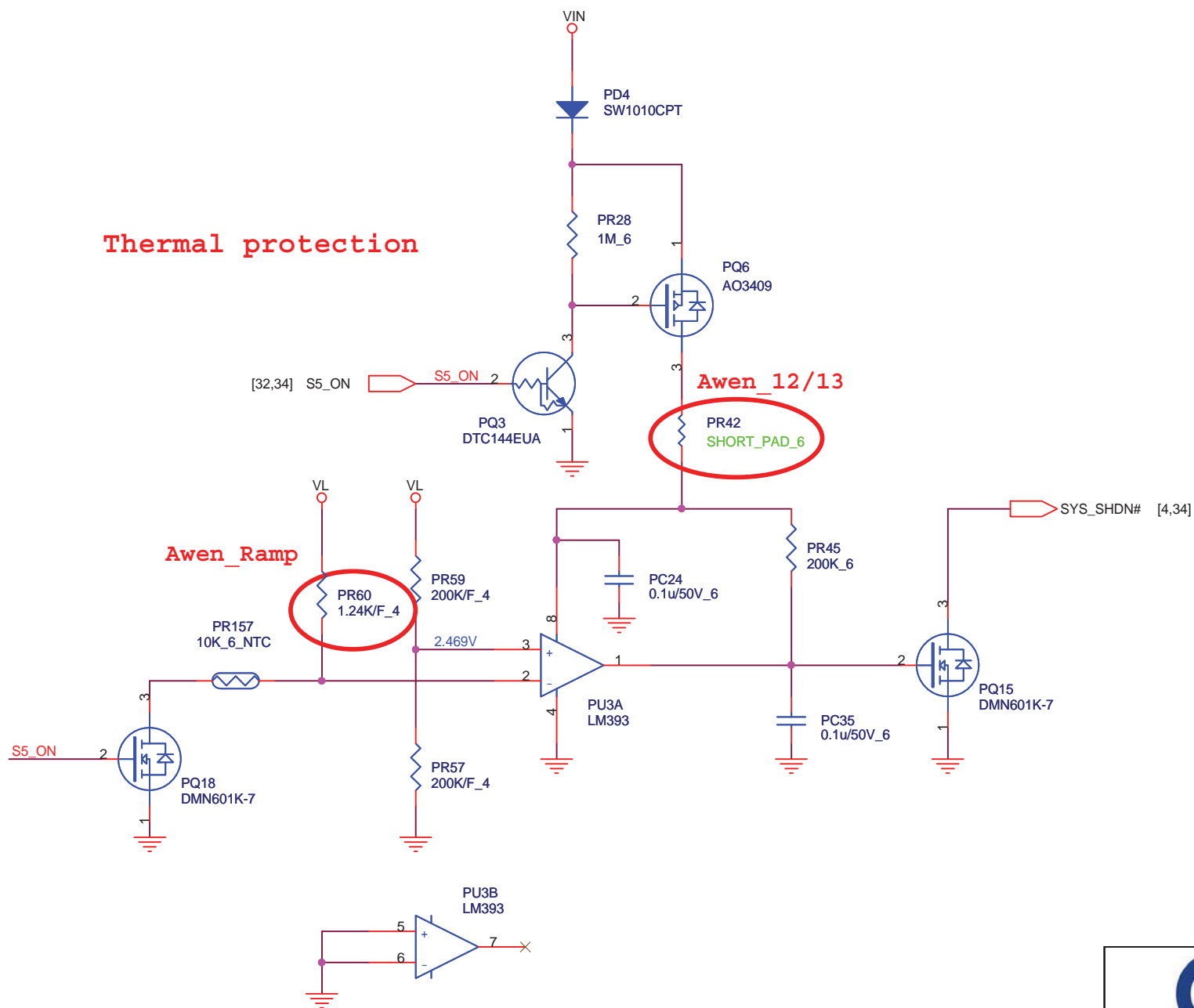
Quanta Computer Inc.

PROJECT : ZRJ

Size	Document Number	Rev
	VCCSA(TPS51461)/+1.8V(HPA00835)	1A
Date:	Saturday, January 22, 2011	Sheet 39 of 41



Thermal protection



For EC control thermal protection (output 3.3V)



Quanta Computer Inc.

PROJECT : ZRJ

Thermal protect

Size	Document Number	Rev 1A
Date: Saturday, January 22, 2011	Sheet 41 of 41	

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